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**Semiclassical Monte Carlo Simulation of
Nano-scaled Semiconductor Devices**

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**Semiclassical Monte Carlo Simulation of Nano-scaled Semiconductor
Devices**

by

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Dedication

To my parents, Sipra Ghosh and Manash K. Ghosh

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As the channel lengths of MOSFETs are being scaled down, the focus is on replacing silicon by high mobility channel materials, such as Ge and III-V semiconductors. This is because mobility and saturation velocity determine the on current of short channel MOSFETs. However, a priori, it is not possible to determine the material that will maximize the ratio of ON current to OFF current. Hence it is interesting to perform simulations to compare the performance of various semiconductor devices with their silicon counterparts.

In this work, a semiclassical Monte Carlo simulator, Monte Carlo University of Texas (MCUT), has been used and modified to handle Ge and III-V MOSFETs. It is capable of handling full bandstructure and incorporates various scattering models, including, inelastic acoustic phonon scattering with longitudinal and transverse modes, optical phonon scattering, impact ionization, ionized impurity scattering, surface

roughness scattering, remote Coulomb, remote surface roughness scattering and polar optical phonon scattering.

Quantum correction in the inversion layer is taken into account in the form of a modified potential that reproduces the correct concentration of carriers. Germanium N- and PMOSFETs and GaAs and InP NMOSFETs seem to perform worse than their silicon counterparts when the saturation currents are compared at the same gate overdrive. The results on GaAs and InP NMOSFETs are considered preliminary at this stage.

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Chapter 1: INTRODUCTION

As the dimensions of semiconductor devices are being scaled down aggressively to reduce size and cost, channel mobility engineering seems to offer the best prospect of improved performance of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). In fact, new materials with higher effective mobility of electrons and holes than that of Si are already being used to increase the drive currents in MOSFETs. These materials are either alloys of Si and Ge ($\text{Si}_x\text{Ge}_{1-x}$) or often strained Si layers built on those alloys. Recently, there has been tremendous interest in III-V semiconductors like InP, InSb, GaAs etc. as possible replacements for Si in modern IC technology. However, how some of these materials will perform in short channel MOSFETs is not obvious. In addition, advantages to the ON current gained from mobility alone may be deceiving since the OFF current depends, among other factors, on the band gap.

With the advent of high- κ dielectrics and their successful combination with Ge channels, the longstanding obstacle of the absence of a stable oxide in Ge technology has also been overcome. Motivated by these multiple considerations, recently, N- and P-MOSFETs in bulk Ge have been successfully fabricated by several experimental groups [Sha02],[Chu02] with substantial improvements in electron and hole mobilities. Although bulk Ge has higher carrier mobilities than bulk Si, it is not clear if it will have any advantage over Si in terms of drive current in sub-100nm MOSFETs. Surface roughness scattering and quantum confinement effects within the channel may affect the relative mobility advantages of one material to the other. Also, the saturation velocities of electrons and holes in Ge are smaller than in Si.

Hence, it is interesting to investigate the potential performance benefits of Ge over Si for short channel MOSFETs via simulation where individual contributions to device behavior can be more readily isolated and especially since the role of mobility in determining the ON current of short channel MOSFETs is not obvious. Addition of biaxial strain in Ge breaks the degeneracy of the hole bands and improves the hole mobility compared to unstrained Ge. This increased mobility will, hopefully, get reflected in higher drain current in nanoscale PMOSFETs. Furthermore, with scaling of the oxide thickness in MOSFETs, new scattering mechanisms, such as, remote surface roughness and remote Coulomb scattering, become important in controlling channel mobility and hence it is interesting to investigate the performance degradation of Ge MOSFETs due to these scattering mechanisms as well.

Recently, there have been reports of some experimental and theoretical (in the ballistic limit) studies, [Rah03][Phu03][Low03], of the mobility and drive current enhancements of unstrained and strained Ge channel MOSFETs over Si MOSFETs. Several experimental and theoretical studies have also been performed to understand the nature and strength of the mobility degrading mechanisms in thin dielectrics (with or without high- κ) on Si and Ge N- and PMOSFETs [Liu87],[Luj03],[Sai02]. In addition to Ge, III-V semiconductors, such as, InP, GaAs etc. are particularly interesting because they have substantially higher electron mobilities than that of Si. However, their densities of states are lower and hence, it is not obvious if there will be any enhancement in the saturation current of short channel MOSFETs. Several experimental and theoretical studies have been made on III-V semiconductor devices. In [Che84], a self-aligned recessed gate InP MESFET with high transconductance has been described. In another interesting work, [Dat05], a 85 nm gate length enhancement and depletion mode InSb quantum well transistor suitable for high speed and very low power logic applications has

been demonstrated. In [Guo04], properties of wurtzite GaN MESFETs of 0.4 μm gate length have been studied by two dimensional fullband Monte Carlo approach and its potential as a high frequency and high power device has been reported. In another study, [Her05], Monte Carlo simulations are performed on nanoscale InSb FETs and the effect of impact ionization on the high speed performance of these MOSFETs have been investigated.

However, there have been no studies on nanoscale Ge or III-V MOSFETs using semiclassical Monte Carlo method taking into account full band structure and scattering, high energy carriers and non-local field effects. In this proposal, we attempt to address the above mentioned issues through semiclassical Monte Carlo simulation.

1.1 ORGANIZATION OF THE DISSERTATION

The aim of this work is to develop a semiclassical Monte Carlo simulation tool capable of simulating short channel length MOSFETs with alternative channel materials, such as, Ge and III-V semiconductors (e.g. InP, GaAs etc.) and compare with their Si counterparts. This dissertation consists of nine chapters discussing the basic theory of semiclassical Monte Carlo simulation, the modifications needed to study alternative materials and the results of the device simulation.

In Chapter Two, we discuss the theory of semiclassical Monte Carlo simulation, discussing, in particular, its advantages over other classical device simulators based on drift-diffusion or hydrodynamic equations. We also discuss the methodology by which the simulator can be used to study alternative channel materials.

Chapter Three contains a discussion of unstrained Ge N and PMOSFETs and comparison with their Si counterparts. We first discuss the methodology of extraction of

various parameters used in the scattering models in Ge MOSFET simulation. Presenting the results of the device simulation we discuss why Ge MOSFETs perform worse than Si MOSFETs .

In Chapter Four, we consider strained Ge PMOSFETs. Biaxial strain along the (001) plane increases hole mobility of Ge and consequently higher ON current. We discuss the method of extracting surface roughness parameters of strained Ge and the comparative results between strained and unstrained Ge PMOSFETs.

Chapter Five consists of a discussion of high-k on Ge MOSFETs. We discuss the issue of mobility degradation due to high-k and the manner in which this degradation can be modeled within the framework of semiclassical Monte Carlo by considering additional scattering mechanisms in high-k dielectrics. The degradation in ON current due to these additional scattering mechanisms in high-k is explained.

Chapter Six consists of a discussion of the effect of channel length reduction on the ON currents of Ge PMOSFETs. It is demonstrated that the strain- induced enhancement of the ON current decreases as the channel length is reduced and reason for the reduction is explained.

In Chapter Seven, we consider, as an aside, the orientation dependence of ON currents in Si NMOSFETs and explain the observed dependence on the surface orientation from the point of view of differential carrier occupation among the six valleys in the conduction band of Si.

Chapter Eight consists of a discussion of III-V semiconductors. A brief overview of the importance of III-V semiconductors, such as, InP, GaAs etc. in modern IC technology is followed by a study of bandstructure and low field mobilities in some of these semiconductors. We present preliminary results of comparative device simulation

between InP, GaAs and Si NMOSFETs and try to explain the observed degradation in ON current in InP and GaAs NMOSFETs as compared to their Si counterparts.

In Chapter Nine, we conclude by giving a summary of already accomplished work and recommend future work.

Chapter 2: SEMICLASSICAL MONTE CARLO

The goal of semiconductor simulation is to solve the Boltzmann transport equation. In recent years, there has been significant progress in numerical device simulation with the focus changing from simple drift diffusion models to more computationally and physically intensive approaches, such as, the semiclassical Monte Carlo simulation. The drift diffusion approach models carrier transport by solving the continuity equation for electrons and holes (by taking the first moment of the Boltzmann transport equation) according to the following equation

$$J_n = nq\mu_n E + qD_n \nabla n \quad (2.1)$$

where the current density J_n depends on the local values of mobility μ_n and diffusivity D_n . E and n denote the electric field and charge density, respectively. In very short channel devices this is no longer a valid assumption and hence drift diffusion equations fail to capture nonlocal effects like velocity overshoot [Bac85]. An improvement over the drift diffusion equation is made by incorporating higher moments of the Boltzmann transport equation, as in the hydrodynamic equations [Bac85]. Although this takes care of some of the nonlocal effects absent in drift diffusion simulations, it requires some simplifying assumptions about the energy relaxation times which may not hold in short channel devices.

The Monte Carlo approach [Jac83] solves the Boltzmann transport equation directly and hence is the best available tool to study transport in short channel devices where nonlocal field effects cannot be neglected. It is a statistical numerical approach to

the solution of the Boltzmann equation. It directly simulates the dynamics of charge carriers inside the crystal, so that, while the solution of the equations is built up, any physical information required can be easily extracted. Monte Carlo method with semiconductor transport consists of a simulation of motion of one or an ensemble of electrons/holes inside the crystal, subject to the action of the internal / external forces and of any given scattering mechanisms. The carrier transport is thus a sequence of free flight and scattering events.

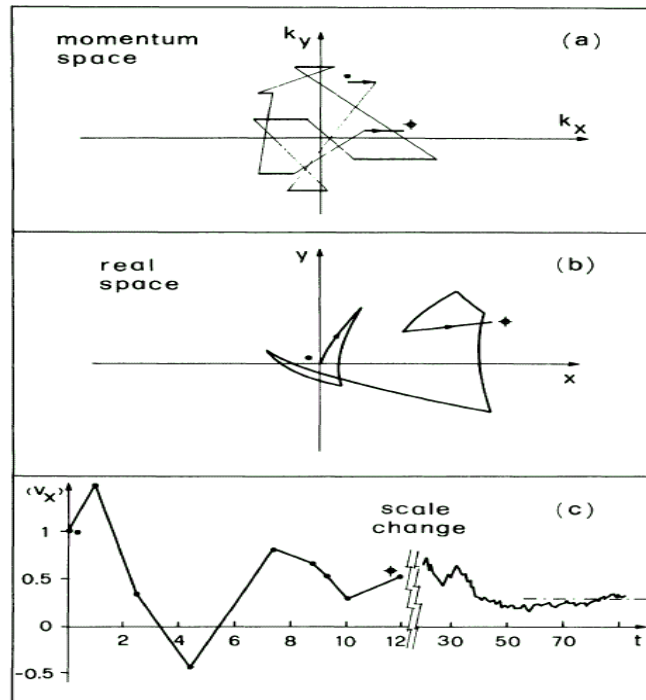


Figure 2.1: The motion of a carrier in momentum space, real space and the dependence of velocity on time in Monte Carlo simulation.

The basic equations are

$$\begin{aligned}\frac{d\vec{r}}{dt} &= \frac{1}{\hbar} \nabla_{\vec{k}} E(\vec{k}), \\ \frac{d\vec{k}}{dt} &= \frac{e}{\hbar} F_{ext}(\vec{r}, t)\end{aligned}\tag{2.2}$$

where $E(\vec{k})$ is the energy of the carrier with momentum \vec{k} , F_{ext} is the electrostatic field at position \vec{r} . Although transport is governed by classical equations of motion, the various scattering mechanisms are obtained by the use of Fermi's Golden rule and hence this method is a mixture of quantum mechanical scattering and classical transport. Hence we use the term 'semi'classical Monte Carlo. Its advantages lie in its comprehensive description of physics, simplicity of implementation, absence of any simplifying assumption on the form of the distribution function in momentum or energy space, the ease of extraction of any physical information from the simulation result and the ability to consider multiple distinct scattering processes. A state of the art Monte Carlo program has been described in [Lau90]. In addition to its semiclassical treatment of transport, the Monte Carlo approach is also flexible enough to incorporate quantum effects which become important for short channel devices through the introduction of quantum corrections to the potential acting on the carriers. In the following, we will describe the particular quantum correction technique used in our Monte Carlo simulator.

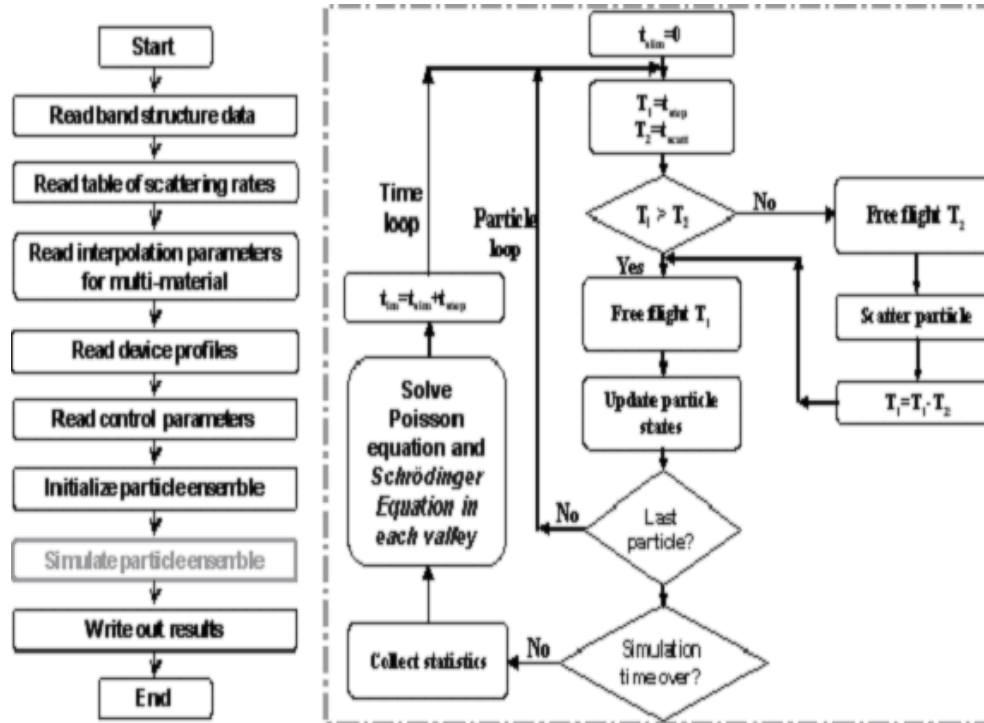


Figure 2.2: Flow chart of the Monte Carlo simulation process.

MCUT is a 2-D Monte Carlo device simulator including full-band structure, self-consistently calculated scattering rates and quantum corrections all within a framework capable of handling with high flexibility and generality various material types and profiles in Si-based MOSFETs in conventional and non-classical CMOS devices as described in detail in [Fan04].

The inputs to MCUT include full band structures and associated phonon scattering rates obtained from preprocessing programs. The band structures are calculated by the pseudopotential or the tightbinding method [Che76][Vog83]. We first describe these bandstructure calculation techniques.

2.1 BANDSTRUCTURE

The bandstructure calculation methods fall broadly into two categories, the first principles method like the density functional theory and the empirical methods like the empirical pseudopotential and tightbinding methods. Empirical methods are simpler, require less computation time but the parameters are adjusted to fit experimental data and hence limited in usage.

2.2 EMPIRICAL PSEUDOPOTENTIAL THEORY

The empirical pseudopotential method was developed in the 1960's, [Phi58],[Phi59],[Kle60], as a way to solve Schrodinger's equation for bulk crystals without knowing exactly the potential experienced by an electron in the lattice. Since electrons interact with the crystal lattice, an electronic band structure calculation is a many-body problem. Although other methods existed at the time for approximating

electronic band structures, the pseudopotential method gives surprisingly accurate results considering the computing time and effort involved. The basic scheme is to assume that the core electrons are tightly bound to their nuclei, and the valence and conduction band electrons are influenced only by the remaining potential. Since the potential can be Fourier expanded in plane waves, an eigenvalue equation for determining an energy-wavevector (E - \mathbf{k}) relationship can be established. Although the Fourier coefficients for the potentials are not known, they can be empirically determined for a given crystal by fitting calculated crystal parameters to known measurements. Cohen and Bergstresser followed these steps to determine band structures of several diamond and III-V zincblende structures [Coh66]. The general form of the pseudopotential is given in [Fri89] and is parametrized as

$$V(q) = \frac{a_1(q^2 - a_2)}{e^{a_3(G^2 - a_4)} + 1} \left[\frac{1}{2} \tanh \left[\frac{a_5 - q^2}{a_6} \right] + \frac{1}{2} \right], \quad (2.3)$$

where $V(q)$ is the pseudopotential in reciprocal vector q . The parameters are then fitted to bulk band structures of the given semiconductor systems. Here $V(q)$ is normalized by the cell volume and the tanh part ensures a fast cutoff for large values of q . The parameters $a_1 - a_6$ for Si and Ge are listed in Table 2.1 in atomic units.

	a_1	a_2	a_3	a_4	a_5	a_6
Si	106.0686	2.2278	0.6060	-1.9720	5.0	0.3
Ge	54.4512	2.3592	0.7400	-0.3800	5.0	0.3

Table 2.1: The pseudopotential parameters for Si and Ge.

2.3 EMPIRICAL TIGHTBINDING

The simplest explicit electronic structure calculation is the “empirical tight-binding (ETB) approximation”, in which we imagine that the electronic eigenstates can be represented by a linear combination of atomic orbitals, $|\psi_i\rangle = \sum_{\mu} a_{\mu}^i |\mu\rangle$ where $|\mu\rangle$ is a site-orbital index and i indexes the state (eigenvector). This method enables the calculation of an approximate one-body Hamiltonian matrix, whose eigenvalues are taken to approximate the allowed electronic energies and the eigen (envelope) functions for the crystal. In the usual implementation of ETB calculations, the basis is taken to be orthonormal. Also, most ETB Hamiltonians include interactions only with nearest neighbors and include only two-center contributions. In the following, we outline the implementation of an ETB calculation.

We begin by considering a supercell model (large unit cell with periodic boundary conditions) of an amorphous solid with N atoms and atomic coordinates $\{R_i\}_{i=1}^N$ and three lattice vectors specifying the periodic boundary conditions. We can view the $\{R_i\}_{i=1}^N$ as specifying a set of “basis vectors” for a crystal with a very large and complex unit cell. Next, we set up the Hamiltonian matrix $H_{\mu\nu} = \langle \mu | \hat{H} | \nu \rangle$ where \hat{H} is the Hamiltonian operator and $|\mu\rangle$ are a set of orbitals (typically s,px,py,pz for a column IV material) centered on each atom. For the purpose of calculating the matrix elements, it is convenient to work with “molecular coordinates” specifying the interatomic hopping. These are V_{ss} , V_{sp} , V_{pp} , chemistry nomenclature for an sp^3 model. Though this generates the valence band structure quite well it fails to generate the conduction band structure. It has been shown in [Ric87] that the unoccupied atomic d orbitals contribute the d symmetry character in the charge density at X, and L points of the conduction band and hence it is necessary to include d states and s^* states. In this work, Staele and Vogl’s

[Vog92] tightbinding code has been used with $sp^3s^*d^5$ basis and the onsite energies and coupling parameters are provided by [Jan98]. Explicit forms for the distance dependence of these interactions are given as a generalization to Harrison's d^{-2} law in [Ren82]. The H matrix eigenvalue problem then reads $H|\psi_i\rangle = \varepsilon_i|\psi_i\rangle$, the usual orthogonal eigenvalue problem, where the electronic eigenvalues are supposed to be approximated by ε_i . For electronic state density calculations an exact diagonalization of H is sufficient.

2.4 SCATTERING

The carriers during motion are subject to scattering from the lattice vibrations, ionized impurities or the roughness of the oxide-channel interface causing an alteration of their momentum and velocity. Inelastic scattering also degrades the energy of carriers. In MCUT we consider phonon, impact ionization, ionized impurity, surface roughness, remote surface roughness, remote Coulomb scatterings, and polar optical phonon scattering. The scattering rates are calculated by Fermi's Golden rule.

The scattering rate of carriers with phonons [Wan93] is given by the following expression

$$P_{\eta,\nu}(k) = \sum_o \frac{1}{(2\pi)^3} \int_{BZ} \frac{\pi}{\rho\omega_\eta(q)} \Delta_{\nu,\nu'}^2(q) |g(q)|^2 \delta[E_{\nu'}(k') - E_\nu(k) \pm \hbar\omega_\eta(q)] (N_q + \frac{1}{2} \pm \frac{1}{2}) \quad (2.4)$$

where k () and k' (') are the initial and final carrier momenta (band indices), respectively, η denotes the phonon mode (both acoustic and optical), $\Delta_{\nu,\nu'}(q)$ the coupling constants (deformation potentials), $\hbar\omega_\eta(q)$ and N_q are phonon energy and

occupation number, respectively and the upper and lower signs denote phonon absorption and emission. $g(q)$ denotes the overlap integral and is given by

$$g(q) = \frac{3}{(qR_{WS})^3} [\sin(qR_{WS}) - qR_{WS} \cos(qR_{WS})] \quad (2.5)$$

where R_{WS} is the radius of the spherical Wigner-Seitz cell [Zim60]. The acoustic phonon coupling constants are taken to be proportional to the phonon momentum ($\Delta_{\nu,\nu'}(q) \sim q\Delta_{\nu,\nu'}$) and the optical phonon coupling constants are taken to be independent of the phonon momenta. The coupling (deformation) potentials are obtained by fitting to bulk velocity-field and energy-field relationships.

The ionized impurity scattering can be implemented by the Brooks Herring [Bro51] or Conwell Weisskopf [Con50] method. The problem of vanishing mobility in the presence of the long range Coulomb force due to ionized impurities is circumvented in the Brooks Herring technique by taking into account the screening due to other carriers while in the Conwell Weisskopf technique the range of the Coulomb potential is limited to the inter-impurity spacing thereby taking into account the effect of other scattering centers. While the Brooks Herring technique is preferred over the Conwell Weisskopf, it fails at low temperatures and high concentrations. Ridley [Rid77] generalized the two techniques by considering both screening and a short range force thereby circumventing the above problem. We use Ridley's scattering rate in MCUT. Empirical parameters in the Ridley model are adjusted to obtain close agreement with the experimental mobility versus concentration data for holes and electrons [Sze47].

Impact ionization becomes a dominant scattering mechanism at high energies. It is modeled by a multi-threshold Cartier like formula [Car93], in general, with the ionization rate being given as

$$\frac{1}{\tau_{ii}(E)} = \sum_{i=1}^n \theta(E - E_{th}^{(i)}) \cdot P^{(i)} \cdot \left(\frac{E - E_{th}^{(i)}}{E_{th}^{(i)}} \right)^{3.5} \quad (2.6)$$

where E is the electron energy, θ is a step function and $E_{th}^{(i)}$ are the threshold energies. The threshold energies are obtained in our case by matching with the experimental impact ionization rate versus field data and mentioned in subsequent chapters. The roughness of the oxide-channel interface causes a perturbation of the potential caused by the gate electrode and hence induces scattering of carriers in the channel. Hence the carrier mobility is degraded compared to bulk by surface roughness scattering. The surface roughness can be characterized by a correlation length L , an rms value of roughness ΔZ and is given by the formula [Jal96],[Goo85],[Yam96]

$$S_{SR}(E) = C_{SR} \cdot D(E) \cdot L^2 \cdot \Delta Z^2 \cdot E_{eff}^\alpha \cdot e^{-\frac{2m_{dos}L^2E}{\hbar^2}} \quad (2.7)$$

where E is the carrier energy, $D(E)$ is the density of states, E_{eff} is the carrier concentration weighted vertical field and m_{dos} is the density-of-states effective mass (for the combined light hole and heavy hole bands and for the individual valleys for the electrons). L , ΔZ and α are fitting parameters obtained via fits to experimental surface mobility data in the case of Si and Ge holes. At higher fields, as was suggested in [Rav00], a dissipation mechanism is provided. This aspect of surface roughness scattering is treated similar to an optical phonon which is inactive at low energies and gradually kicks in at higher

energy values. (Here it should be noted that an effect of quantum confinement near the surface is to actually increase phonon scattering so that there is a physical basis for this phonon-like contribution to surface roughness scattering, [Yam96]). The scattering rate for surface phonon scattering is given as

$$S_{\text{surface-phonon}} = RE_{\text{eff}}^{\beta} \quad (2.8)$$

where R and β are tunable parameters.

As the channel lengths of MOSFETs are being scaled down, so also must the oxide thickness in order to allow sufficient gate control over the channel. However, with conventional dielectrics like SiO_2 reduction in the oxide thickness causes high gate leakage current and degrades the input impedance of MOSFETs. Therefore, high dielectric constant (κ) materials are used between the gate and the oxide. This allows for the reduction the equivalent thickness of the oxide while keeping the physical oxide thickness high enough to reduce leakage currents. However, high- κ reduces the mobility of carriers in the channel. Recently several experimental and theoretical studies have been performed to understand the nature and strength of the mobility degrading mechanisms in thin dielectrics (with or without high- κ) on Si and Ge N- and PMOSFETs [Gam03],[Rol03]. Of these, we implemented remote surface roughness and remote Coulomb scattering in MCUT. We implement remote surface roughness scattering along the lines of [Liu87] and mention the rate formula below,

$$S_{\text{remote-surface-roughness}} = \text{CRSR}(L_1 D_1)^2 \sqrt{E} \int_0^{\pi} \left(1 + \frac{1}{qt_{\text{ox}}}\right)^2 e^{-2 \cdot q \cdot t_{\text{ox}}} \left(\frac{b}{b+q}\right)^6 e^{-q^2 L_1^2 / 4} \sin \theta d\theta \quad (2.9)$$

where θ is the angle between the initial (k) and final (k') carrier wave vectors, q is the magnitude of $q = k - k'$ and is given by,

$$q = 2 \sqrt{\frac{2mE}{\hbar^2}} \sin \frac{\theta}{2} \quad (2.10)$$

with m being the combined density-of states mass of the heavy and light holes and is taken to be $0.43m_0$ where m_0 is free electron mass. E is the carrier energy, t_{ox} is the thickness of the dielectric and b is a measure of the average distance of carriers from the dielectric-channel interface and is given by

$$b = \left(\frac{33\pi em}{\hbar^2} E_{eff} \right)^{\alpha_1} \quad (2.11)$$

where E_{eff} is the effective electric field and e is the free electron charge. L_1, D_1, α_1 and CRSR are tunable parameters.

Remote Coulomb scattering has been implemented along the lines of [Luj03] and the rate formula is given by

$$S_{remote-coulomb} = Coulomb \sqrt{E} \int_0^\pi \frac{1}{q^2} \left(\frac{b}{b+q} \right)^6 \left[\frac{a_1^2}{4q-q_1} A - \frac{2a_1 b_1}{2q-q_1} B + \frac{b_1^2}{q_1} C \right] \sin \theta d\theta \quad (2.12)$$

where

$$A = e^{-(4q-q_1)t_s} - e^{-(4q-q_1)t_e}, \quad B = e^{-(2q-q_1)t_s} - e^{-(2q-q_1)t_e}, \quad C = e^{q_1 t_s} - e^{q_1 t_e} \quad (2.13)$$

$$a_1 = 1 - \beta^2 \chi(q), \quad b_1 = \beta(1 - \chi(q)), \quad \chi(q) = \frac{1 - e^{-2qt_{ox}}}{1 - \beta^2 e^{-2qt_{ox}}}, \quad (2.14)$$

and

$$\beta = \frac{\mathcal{E}_{channel} - \mathcal{E}_{high-\kappa}}{\mathcal{E}_{channel} + \mathcal{E}_{high-\kappa}}. \quad (2.15)$$

The fixed charge density in the dielectric is assumed to follow a Gaussian distribution extending from t_s to t_e and is of the following form

$$N_{fixed-charge}(z) = N_{ox} e^{-q_1 z} \quad (2.16)$$

where $q_1 = 1 \times 10^9 \text{ cm}^{-1}$, $N_{ox} = 1 \times 10^{14} \text{ cm}^{-2}$ and z denotes the distance of the fixed charge in the dielectric from the channel-dielectric interface. The quantities Coulomb, t_s and t_e are tunable parameters which, along with the parameters mentioned earlier for remote surface roughness scattering, have been tuned to match the experimental and MCUT results on the dependence of mobility-effective field data on the thickness of the dielectric.

For III-V semiconductors, the bond between the two dissimilar atoms gives rise to a dipole moment. As the atoms vibrate the dipole moment changes and the carriers feel the electric field of the changing dipole and scatter. This is polar optical phonon scattering. The term ‘polar’ refers to the dipole moments created when the oppositely charged ions move in the opposite direction as occurs for longitudinal optical phonons. The dipole moments created interact with the charge of the carriers. The polar optical phonon scattering rate is given by the following expression [Jac90]

$$S_{polaroptical} = \frac{e^2 \sqrt{m\omega_{op}}}{\sqrt{2}C\hbar} \left(\frac{1}{k_{\infty}} - \frac{1}{k_o} \right) \frac{1+2\alpha E'}{\sqrt{\gamma(E)}} F_0(E, E') \left[N_q + \frac{1}{2} \pm \frac{1}{2} \right] \quad (2.17a)$$

for $E > \hbar\omega_{op}$ and

$$S_{polaroptical} = 0 \quad (2.17b)$$

for $E < \hbar\omega_{op}$, where

$$F_0(E, E') = \frac{1}{C} \left\{ A \ln \left| \frac{\sqrt{\gamma(E)} + \sqrt{\gamma(E')}}{\sqrt{\gamma(E)} - \sqrt{\gamma(E')}} \right| + B \right\} \quad (2.18)$$

and

$$\begin{aligned} A &= \{2(1+2\alpha E)(1+\alpha E') + \alpha[\gamma(E) + \gamma(E')]\}^2 \\ B &= -2\alpha\sqrt{\gamma(E)\gamma(E')}\{4(1+\alpha E)(1+\alpha E') + \alpha[\gamma(E) + \gamma(E')]\} \\ C &= 4(1+\alpha E)(1+\alpha E')(1+2\alpha E)(1+2\alpha E') \end{aligned} \quad (2.19)$$

E, E' denote the initial and final energies of the carriers, $E' = E \mp \hbar\omega_{op}$ and upper and

lower signs correspond to emission and absorption respectively. Also

$$\gamma(E) = E(1 + \alpha E) \quad (2.20)$$

where

$$\alpha = \frac{1}{E_g} \left(1 - \frac{m}{m_0}\right)^2 \quad (2.21)$$

is the nonparabolicity factor. m is the effective mass, e the charge on an electron, N_q denotes the carrier occupation number, ω_{op} is the optical phonon energy and k_∞ and k_o denote the high frequency and static dielectric constants respectively.

These full band calculations also allow for consideration of strain induced degeneracy breaking and the associated variations in scattering rates.

The quantum corrections address quantum-confinement induced redistribution of charge carriers in both position (real-space) and among energy valleys (in k-space). The quantum corrections are provided via first matching the classical equilibrium carrier distributions for each energy valley to that obtained quantum mechanically within an effective mass approximation via shifting the energy valley edges in the former. These valley-dependent valley edge shifts are then mapped to the full band structure code via a shift in the overall conduction/valence band edge and an “effective strain” of the semiconductor that reproduces the same valley splitting. Besides avoiding certain computational ambiguities within this full band MC tool for high energy carriers between valleys where the effects of quantum-confinement are neither easily obtained nor of great significance, this approach has the advantage of allowing the use of the pre-calculated self-consistent scattering rates of the (effectively) strained material as well. This approach also allows the effects of (real) strain and quantum confinement to be readily combined into one net effective strain as detailed in [Fan04].

In a device, due to the vertical electric field and the associated quantum well in the inversion layer, the carrier energies are split into discrete subbands instead of a continuous set. This modification of carrier energies is particularly significant for low energy carriers with energies near the band edges, in particular for holes near the Γ point.

Let $E(\vec{k}, z)$ denote the band structure obtained, for holes, from the tightbinding Hamiltonian. The band structure has a dependence on z , the position normal to the interface due the band discontinuity at the oxide - channel interface. At the Γ point, denoted by wavevector \vec{k}_o , for each of the heavy hole, light hole and split off bands, the one dimensional effective mass Schrodinger equation normal to the interface (taken in the z direction) can be written as

$$-\frac{\hbar^2}{2} \frac{\partial}{\partial z} \left[\frac{1}{m_{z,l}(z)} \frac{\partial}{\partial z} \psi_{l,i}(x, z) \right] + [E(\vec{k}_o, z) + eV(x, z)] \psi_{l,i}(x, z) = E_{l,i}(x) \psi_{l,i}(x, z) \quad (2.22)$$

where $m_{z,l}$ denotes the effective mass of heavy hole, light hole and split off band respectively for $l=1,2$ and 3 , $V(x,z)$ denotes the electrostatic potential and $\psi_{l,i}(x, z)$, the wave functions for each of the hole bands. The equilibrium quantum mechanical hole density for each hole band is given, in the Boltzmann approximation by

$$\begin{aligned} n_{qc,l}(x, z) &= \sum_i |\psi_{l,i}(x, z)|^2 \cdot \int_0^\infty g_{2D}(E_{\parallel}) \cdot e^{-\frac{E_{\parallel} + E_{l,i}(x)}{K_B T}} dE_{\parallel} \\ &= \sum_i |\psi_{l,i}(x, z)|^2 \cdot \frac{m_{dos}}{\pi \hbar^2} \cdot e^{-\frac{E_{l,i}(x)}{K_B T}} \end{aligned} \quad (2.23)$$

where we measure all energies with respect to the Fermi energy. The quantum corrected band structure, $E_{qc}(\vec{k}_o, x, z)$, is then defined as the one that produces the same equilibrium hole density for each hole band at the Γ point,

$$n_{qc,l}(x,z) \equiv N_l \cdot e^{-\frac{E_{qc}(\vec{k}_0, x, z) + eV(x, z)}{K_B T}} \quad (2.24)$$

where N_l is the effective density of states per hole band. It should be noted that this method of calculating quantum correction uses the density of states mass of the holes and is valid at and near the Γ point. In order to obtain a complete quantum corrected band structure for all wave vectors \vec{k} , we simply add the difference ΔE , between the quantum corrected energy and the uncorrected energy at the Γ point, to the original uncorrected band structure energies for all values of \vec{k} .

The particles in the Monte Carlo ensemble then move under the influence of the quantum corrected band structure. The motion of the particles changes the local concentration and, by Poisson equation, also the potential $V(x,z)$ which in turn changes the wave functions calculated from the Schroedinger equation and results in a new quantum corrected band structure used to move the particles and the process is repeated till self consistency is reached between the particle concentration and the potential.

Chapter 3: UNSTRAINED GE N- AND PMOSFETs

3.1 MOTIVATION

Recently, there has been significant interest in Ge channel MOSFETs as possible replacements for Si channel devices. Bulk Ge has two times the low-field electron mobility and four times the hole mobility of bulk Si, suggesting the possibility of increased drive current. However, how this advantage in mobility should translate to improved drive current in sub-100 nm channel length MOSFETs is not completely clear. Surface roughness scattering and differences therein between Si and Ge devices may affect the relative mobility advantages of one material to the other. Also, as pointed out by several experimental groups, [Sha02],[Chu02],[Lee01], Ge devices suffer from high defect densities and interface charges at the oxide-channel interface which can substantially affect the mobilities in these devices. And, of course, the saturation velocities of electrons and holes in Si are respectively higher than those of electrons and holes in Ge. More importantly for the drive currents of deeply scaled devices [Lun97], the thermal velocities of holes, in particular, are similar in Ge and Si, at least as obtained with the bandstructure model we used here [Vog92]. Recently, devices based on Ge have been reported by several experimental groups [Sha02], [Chu02], [Lee01], however improved drive currents have not been exhibited (quite the opposite in fact). It has been speculated that this performance deterioration may result in part due to poor dopant activation in the source and drains of the Ge devices.

Given the above multiple considerations, it becomes interesting to investigate the potential performance benefits of Ge over Si for short channel length MOSFETs via simulation where individual contributions to device behavior can be more readily

isolated. Monte Carlo studies of drift velocities and mobilities of electrons and holes in bulk Ge and Si have been performed [Phu03]. However, there have been very few theoretical studies of Ge P- and N- MOSFETs. In [Low03] and [Rah03], quantum simulations of ultra-thin body, double-gated Ge NMOSFETs were performed using the Non-Equilibrium Green's Function formalism (NEGF) and their performance benefits over Si NMOSFETs were reported. However, these studies did not take into account scattering which is critically related to both mobility and channel injection efficiencies. And, to the best of our knowledge, there has been no theoretical Monte Carlo study of Ge PMOSFETs although they are particularly interesting because an improvement in hole mobility suggests the possibility of comparable drive currents in P- and N- MOSFETs in complementary metal-oxide-semiconductor (CMOS) Ge technology. However, hole transport study is, particularly, very challenging due to the complexity of the valence band structure. In this respect a full-band Monte Carlo study of Ge MOSFETs and including comparison with Si MOSFETs can help bridge the gap in the theoretical understanding of Ge PMOSFETs while shedding useful insights in addition to those obtained from NEGF simulations for electrons via the treatment of scattering. To this end, in this chapter, we present an extension of our semiclassical Monte Carlo simulation tool [Fan04] developed for simulating electron and hole transport in Ge channel devices, and use this tool to study the current voltage characteristics of Ge bulk n- and p- channel MOSFETs and compare the results with those for their Si counterparts. In our simulations, we consider transport including phonon, ionized impurity, surface roughness scattering and impact ionization. Carrier redistribution in real space and among energy valleys (k-space) due to quantum confinement within the inversion layer is addressed via position and valley/band-dependent quantum-corrected potentials.

This chapter is organized as follows. We first summarize the modifications made to the Monte Carlo device simulator “MC University of Texas” (MCUT), used in simulation of Si MOSFETs, to study Ge MOSFETs. We then present the results of our simulations of Ge P- and N- MOSFETs and compare results with those of the Si control devices. We then explain the observed degradation and degree thereof in terms of the various factors addressed above.

3.2 ADAPTATION OF MCUT TO GE MOSFETs

In the following we briefly describe the modifications made to the existing version of MCUT to allow simulation of Ge channel devices. The bandstructure and the phonon scattering rate table are obtained from the same pre-processing programs as in the Si version, with tight-binding and pseudo-potential parameters obtained from [Vog92],[Che76]. With a smaller bandgap, impact ionization becomes an increasingly important phenomenon and influencing the properties of high energy carriers in Ge devices. The deformation potentials for phonon scattering and threshold energies for impact ionization have been simultaneously tuned to obtain reasonable agreement with data from the literature [Fis96], [Yam95], [Sze47], [Jac83]. The data considered include velocity, energy and impact ionization rates versus field for bulk Ge electrons and holes, as shown in Figures 3.1- 3.5. We use a multi threshold Keldysh formula for impact ionization in Ge,

$$\frac{1}{\tau_{ii}(E)} = \sum_{i=1}^n \theta(E - E_{th}^{(i)}) \cdot P^{(i)} \cdot \left(\frac{E - E_{th}^{(i)}}{E_{th}^{(i)}} \right)^{3.5} \quad (3.1)$$

where E is the electron energy, θ is a step function and $E_{th}^{(i)}$ are the threshold energies. The values of $E_{th}^{(i)}$ and $P^{(i)}$ used to study Ge holes are $E_{th}^{(i)} = 1.5, 2.3, 2.7$ and 3.0 eV and $P^{(i)} = 2.3 * 10^{14}, 5.2 * 10^{14}, 9.1 * 10^{15}$ and $13.1 * 10^{15} \text{ s}^{-1}$, respectively for $i = 1, 2, 3$ and 4 . The values used for electron impact ionization are $E_{th}^{(i)} = 1.1, 7.2$, and 24.85 eV and $P^{(i)} = 2.2 * 10^{12}, 2.1 * 10^{18}$ and $2.2 * 10^{12} \text{ s}^{-1}$, respectively for $i = 1, 2$ and 3 . The values of the acoustic longitudinal (Δ_{LA}), acoustic transverse (Δ_{TA}) and optical (Δ_{OP}) deformation potentials used for holes and electrons in this study are given in Table 3.1. (The given values of the deformation potentials and impact ionization parameters, however, are not unique in their ability to match the experimental velocity-field and impact ionization data and other sets of values can be used.)

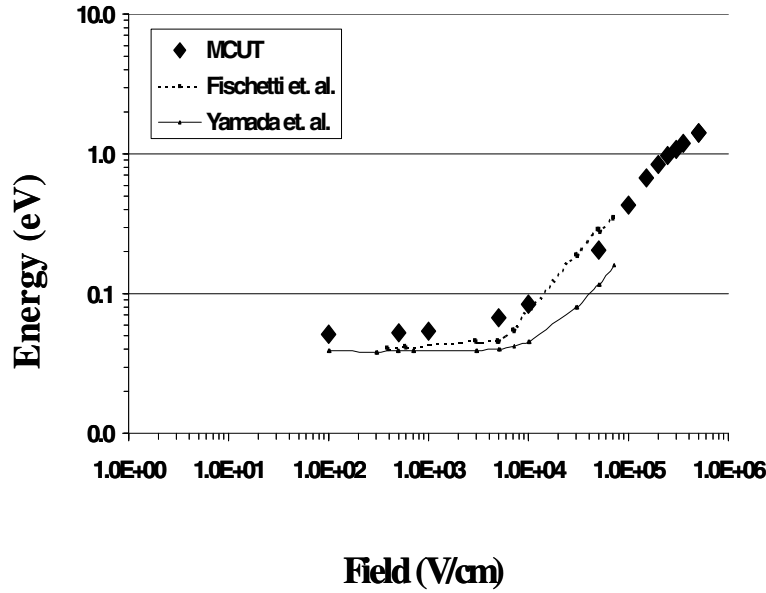


Figure 3.1: Energy versus field for holes in Ge.

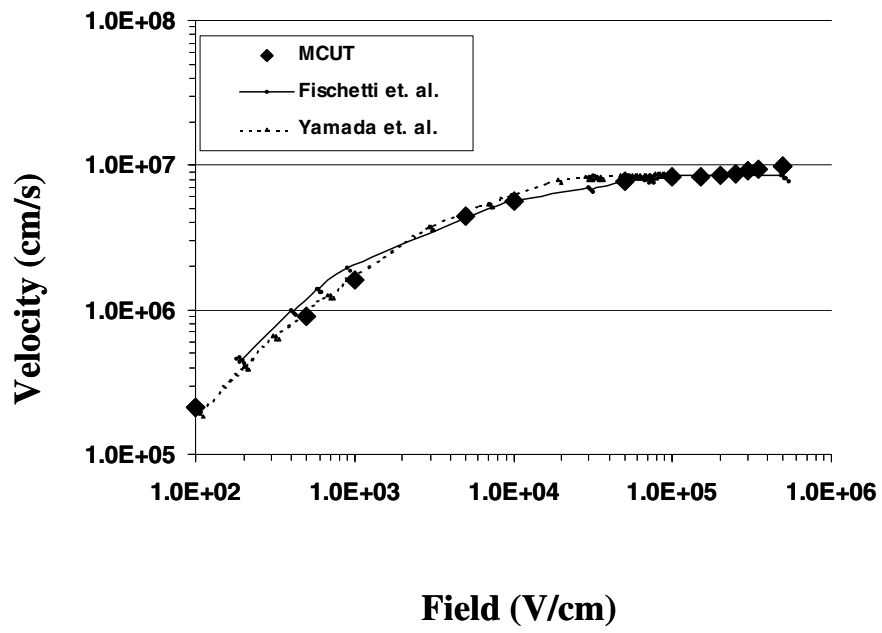


Figure 3.2: Velocity versus field for holes in Ge.

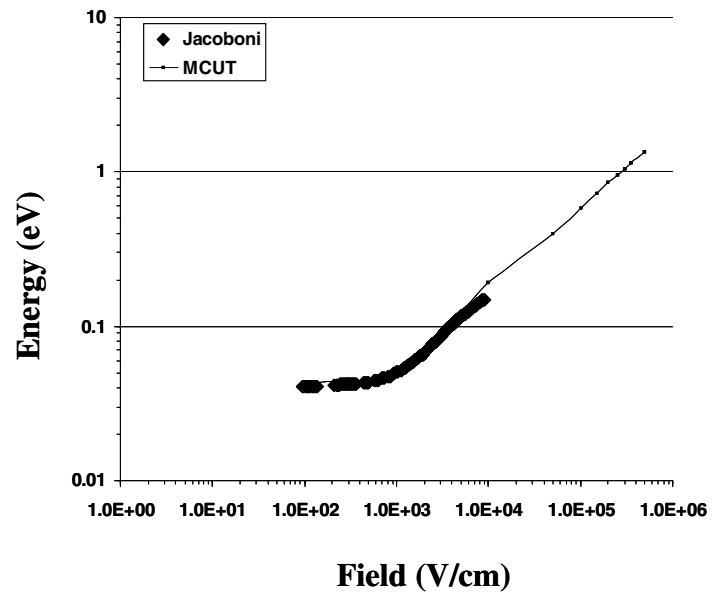


Figure 3.3: Energy versus field for electrons in Ge.

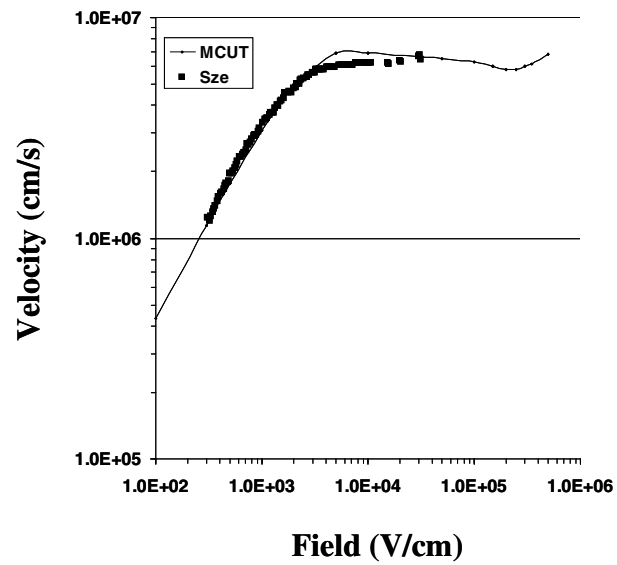


Figure 3.4: Velocity versus field for electrons in Ge.

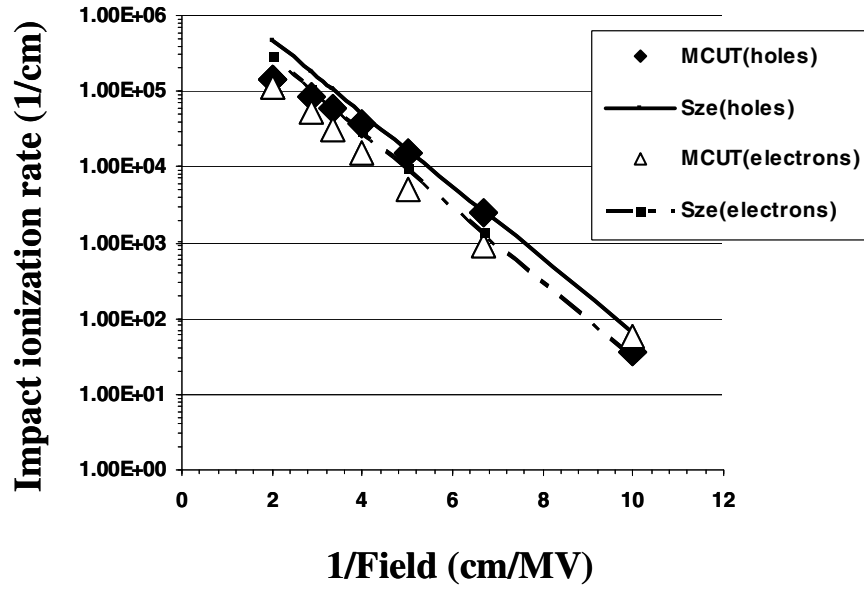


Figure 3.5: Impact ionization rate versus inverse electric field for electrons and holes in Ge.

Deformation potential / band	Δ_{LA} (eV)	Δ_{TA} (eV)	Δ_{OP} (eV/cm)
Holes(all bands)	1.0	1.0	$8.0 \cdot 10^8$
Electrons(all bands)	4.54	2.49	$4.6 \cdot 10^8$

Table 3.1: Deformation potentials for electrons and holes in Ge.

Ionized impurity scattering is modeled along the lines of Ridley's generalized treatment [Car93]. Empirical parameters in the Ridley model are adjusted to obtain close

agreement with the experimental mobility versus concentration data, [Sze47], for electrons and holes in bulk Ge as shown in Figure 3.6.

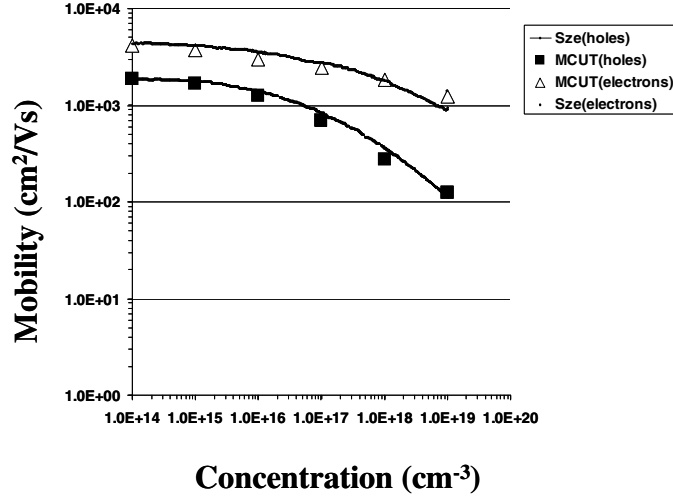


Figure 3.6: Mobility versus acceptor and donor concentrations for holes and electrons in Ge.

Surface roughness scattering is modeled along the lines mentioned in equation 2.7. For (holes) electrons the parameters are adjusted to match experimental mobility versus effective field data in ([Goo85]) [Xia04] for Ge (PMOSFETs) NMOSFETs as shown in Figure (3.7) 3.8. The values of the above parameters obtained for Ge NMOSFETs are $L = 22 \text{ \AA}$, $\bullet Z = 2.01 \text{ \AA}$, $\bullet = 2.0$, and $m_{\text{dos}} = 0.22 m_0$ where m_0 is the free electron mass and for PMOSFETs they are $L = 20 \text{ \AA}$, $\bullet Z = 30.03 \text{ \AA}$, $\bullet = 0.565$ and $m_{\text{dos}} = 0.34 m_0$.

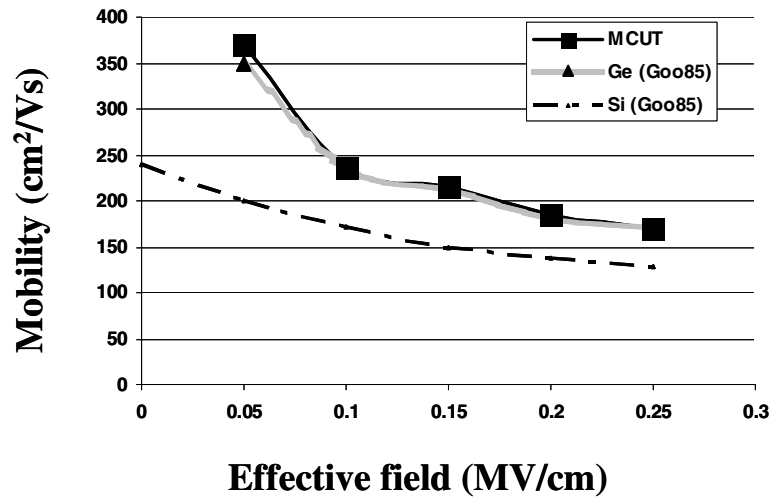


Figure 3.7: Mobility versus transverse effective field for holes in Ge and comparison with Si PMOSFETs.

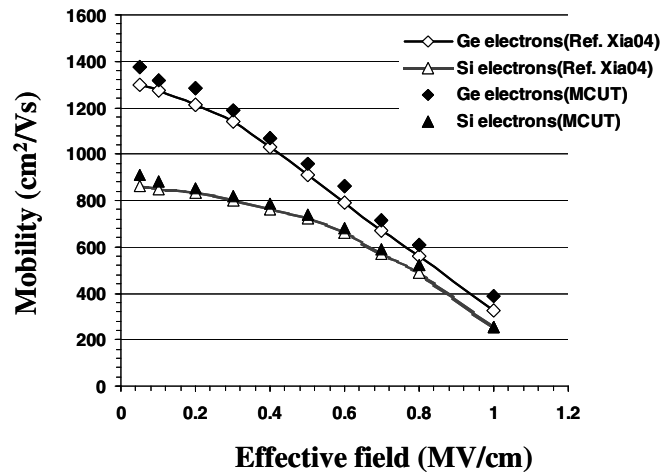


Figure 3.8: Mobility versus transverse effective field for electrons in Ge and comparison with Si NMOSFETs.

The Ge quantization effective mass values used for hole bands to obtain the quantum corrections as outlined above are the 3D density-of-states mass of $0.33 m_0$, $0.043 m_0$ and $0.084 m_0$ for the heavy holes, light holes and split off holes respectively, where m_0 is the free electron mass [Sze47]. For electrons, on a {100} surface plane and energy valleys at the L points along the <111> directions the quantization effective masses used were taken from [Sha03].

3.3 DEVICE SIMULATION RESULTS

Device simulations were performed on 50nm channel length P- and NMOSFETs. These devices were constructed similar to that in [Ant99] and have a 2 nm thick gate oxide, substrate doping of $1 \times 10^{15} \text{ cm}^{-3}$ and with {100} surface orientations and <100> transport directions. For Si MOSFETs SiO_2 is used as the gate oxide and for Ge MOSFETs GeON is used. The p+ (n+ for NMOSFET) source/drain region has a Gaussian distribution with a peak density of $2 \times 10^{20} \text{ cm}^{-3}$ and a p+ (n+) polySi gate of 85nm physical length (with a doping of $2 \times 10^{20} \text{ cm}^{-3}$ and height of 60 nm). Figures 3.9 and 3.10 show the I_d versus V_d curves, for the Ge p- (n-) MOSFET, respectively, and the Si control device at $|V_g - V_t| = 1.0 \text{ V}$. The threshold voltage of the Ge devices were raised to make them equal to those in the Si devices by increasing the channel doping in the Ge devices. For the Ge PMOSFET (NMOSFET) the channel doping has been raised from $1 \times 10^{15} \text{ cm}^{-3}$ to $2.5 \times 10^{18} \text{ cm}^{-3}$ ($3.9 \times 10^{18} \text{ cm}^{-3}$). The degradation in drive current in Ge MOSFETs over Si is clearly evident from figures 3.9 and 3.10. The degradation in on

current (at $|V_d| = 1.2 \text{ V}$) of Ge PMOSFET (NMOSFET) is about 25 % (32 %) as compared to Si.

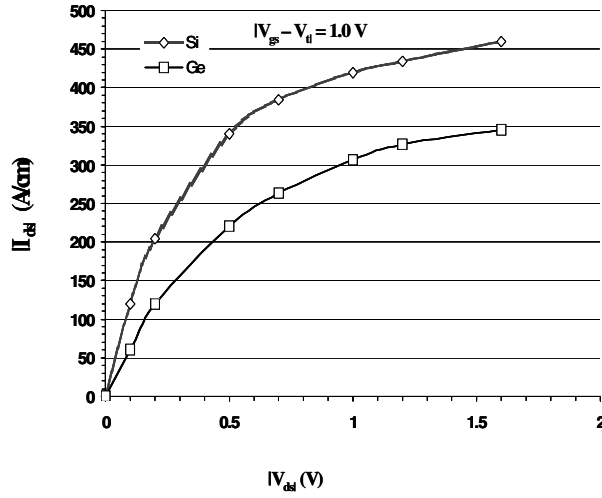


Figure 3.9: Drain current versus drain voltage characteristics for 50nm channel length Ge and Si PMOSFETs with 2nm effective oxide thicknesses. The surface and channel orientations are along $\{001\}$ and $\langle 100 \rangle$, respectively. The values of currents and voltages are negative but absolute values have been plotted.

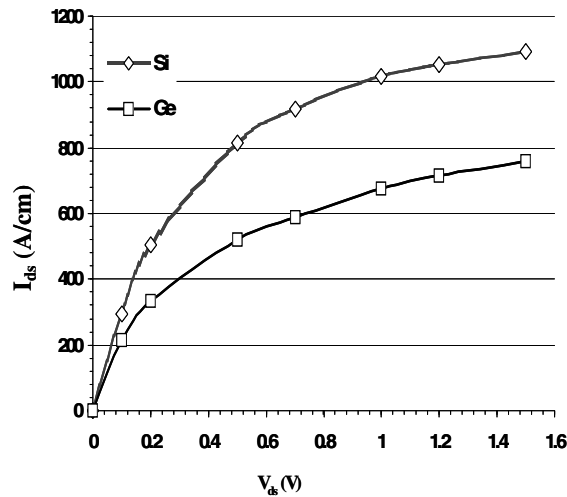


Figure 3.10: Drain current versus drain voltage characteristics for 50nm channel length Ge and Si NMOSFETs with 2nm effective oxide thicknesses. The surface and channel orientations are along $\{001\}$ and $\langle 100 \rangle$, respectively.

Notably, for PMOSFETs, the effective transverse fields corresponding to the peak position of the source drain barrier were 1.01 MV/cm and 1.23 MV/cm, respectively, for the Ge and Si devices under these conditions. The difference in effective fields is due to the differing relative dielectric constants of Ge and Si, 16 and 11.8 respectively. These effective fields correspond to low field mobilities (with channel doping of $2.5 \times 10^{18} \text{ cm}^{-3}$ for Ge and $1 \times 10^{15} \text{ cm}^{-3}$ for Si) of $42.53 \text{ cm}^2/\text{Vs}$ and $68.59 \text{ cm}^2/\text{Vs}$, respectively as obtained for long channel devices at low drain voltages. Much of the mobility advantage of Si comes from the lower channel doping in Si (although Ge has lower effective field and reduced surface roughness). For NMOSFETs, the effective transverse fields corresponding to the peak position of the source drain barrier were 1.06 MV/cm and 1.37 MV/cm, respectively, for the Ge and Si devices under these conditions, again because of the difference in dielectric constants. These effective fields correspond to low field mobilities (with channel doping of $3.9 \times 10^{18} \text{ cm}^{-3}$ for Ge and $1 \times 10^{15} \text{ cm}^{-3}$ for Si) of $329 \text{ cm}^2/\text{Vs}$ and $897 \text{ cm}^2/\text{Vs}$, respectively.

3.4 DISCUSSION

Regarding mobility alone for the moment, we note that with not all that dissimilar conductivity effective masses, particularly for holes, the low field mobility improvement in bulk Ge over Si must be attributed to reduced phonon scattering. In figures 3.11, 3.12 and 3.13 we plot the valence bandstructures of Ge and Si along the {111}, {100} directions and the phonon scattering rates.

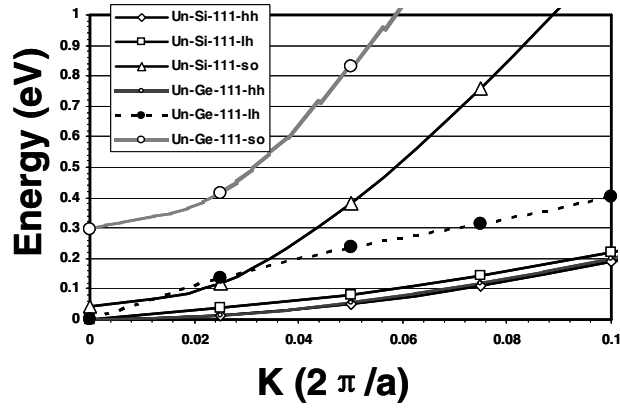


Figure 3.11: Valence bandstructure along the {111} direction for Si and Ge.

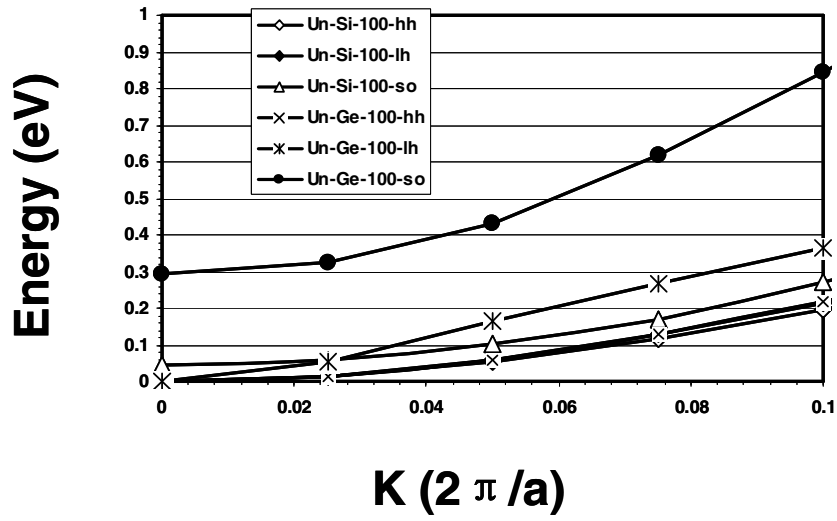


Figure 3.12: Valence bandstructure along the {100} direction for Si and Ge.

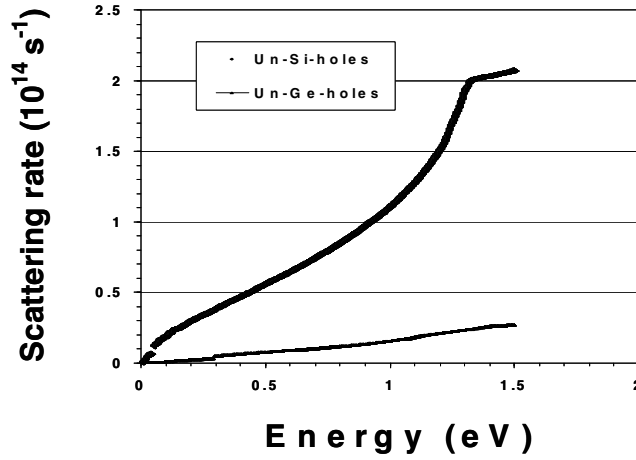


Figure 3.13: Phonon scattering rates for holes in Si and Ge.

However, surface roughness scattering plays a critical role in channel mobilities reducing the relative mobility increase for Ge over Si in the inversion channel as compared to that in bulk. Somewhat mitigating this effect is the reduced effective field in the Ge devices. However, the overriding factor in these simulations is that the channel doping in Ge devices is much higher than in Si devices (in order for both to have the same threshold voltages) so that, all things considered, the relative channel mobilities in Ge is actually less than that of Si at the same $|V_g - V_t| = 1.0$ V.

The decrease in drive current, 25% and 32% for these 50 nm p- and n-channel devices, respectively, is, at least, substantially smaller than the degradation in mobility. As pointed out in [Lun97], the source to channel transition region plays a critical role in determining the saturation drain current for short channel devices. The current decreases with decrease in mobility (since a decrease in low field mobility corresponds to an increase in backscattering from the channel) and thermal injection velocity at the source. It is the latter that limits the injection current in the ballistic limit. For these simulations

of short channel devices and, with nearly equal thermal velocities for holes and electrons for the employed fullband structure, much of the disadvantages of reduced channel mobility of Ge is lost.

Furthermore, Fig. 3.14 compares the velocity profiles along the entire length including the source, the channel and the drain for the Ge and Si 50nm PMOSFETs. Although, as pointed out in [Lun97], increased carrier velocity further down the channel including any velocity overshoot of the carriers does not extend the limit of the saturation current, we point out that the significant velocity overshoot does improve transit times through the device which would be significant for intrinsic switching speed, and in this aspect, Ge has an advantage over Si.

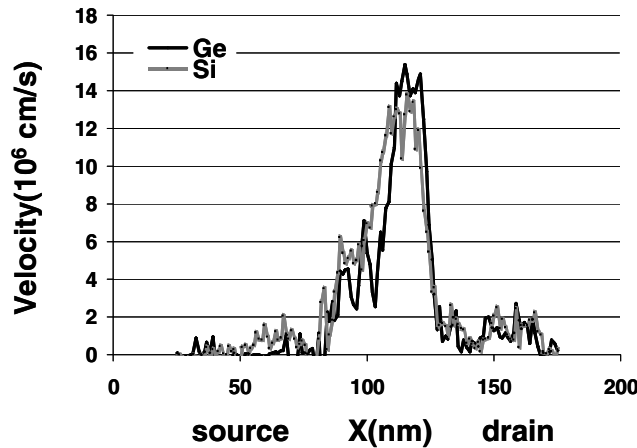


Figure 3.14: Velocity profile from source to drain in 50 nm channel length Si and Ge PMOSFETs. The entire MOSFET extends from 25 to 175 nm. The channel is of effective length 50 nm and extends from about 75 to 125 nm.

Chapter 4: STRAINED GE PMOSFETS

4.1 MOTIVATION

As device dimensions are being reduced to their ultimate limits, new materials with higher effective mobility of electrons and holes than that of Si are being used to increase the drive currents in MOSFETs. These materials are either alloys of Si and Ge ($\text{Si}_{1-x}\text{Ge}_x$) or strained Si layers built on those alloys. The advent of high- κ dielectrics and their successful combination with Ge channels has removed the longstanding obstacle of the absence of a stable oxide in Ge technology. Recently, N- and P- MOSFETs of pure Ge have been successfully fabricated by several experimental groups [Sha02][Chu02] with substantial improvements in hole mobilities. From the fabrication point of view, though, it is most economical to grow a pure Ge layer on a Si substrate with or without a virtual substrate layer with slightly lower composition than pure Ge. The compressive strain induced by the lattice mismatch between the virtual layer and the pure Ge layer reduces interband scattering for holes and hence increases the mobility of the strained Ge PMOSFETs relative to the unstrained case. For NMOSFETs a similar reduction in mobility is not expected as a result of biaxial strain in the plane with normal along $\{001\}$ direction since the four L valleys of the Ge conduction band remain degenerate in energy even after the application of strain. Strained Ge PMOSFETs have been recently reported by several experimental groups [Lee01][Rit03]. The increase in mobility of holes in strained Ge devices results from reduced interband scattering [Sha04]. In [Lee01] strained Ge PMOSFETs have been fabricated on a $\text{Si}_{0.3}\text{Ge}_{0.7}/\text{Si}$ virtual substrate with SiO_2 as gate material and a Si cap layer between the strained Ge channel and the oxide. In

another work, [Rit03], strained Ge PMOSFETs have been fabricated on a $\text{Si}_{0.3}\text{Ge}_{0.7}/\text{Si}$ virtual substrate with TaN/HfO_2 as gate stack and without a cap layer.

Although there have been many experimental works on strained Ge MOSFETs, no theoretical study has so far been attempted. It is, therefore, interesting to investigate the performance benefits, if any, of introducing strain in the Ge layer of nanoscale Ge MOSFETs. In this chapter, we describe a full band Monte Carlo study of strained Ge PMOSFETs and compare with their unstrained Ge counterparts. The mobility versus effective field data in [Rit03] is suitable for simulation using our Monte Carlo simulator since they do not have a Si cap layer on the Ge layer and hence consider only single channel devices unlike the data in [Lee01] which considers dual channel Ge devices. In our simulations, we consider transport including phonon, ionized impurity, surface roughness scattering and impact ionization. Carrier redistribution in real space and among energy valleys (k-space) due to quantum confinement within the inversion layer is addressed via position and valley/band-dependent quantum-corrected potentials.

This chapter is organized as follows: We start with a brief discussion of the modifications made to MCUT to study strained Ge PMOSFETs. Next we present the results of our simulations of strained (Ge on $\text{Si}_{0.3}\text{Ge}_{0.7}/\text{Si}$) Ge PMOSFETs and compare the results with those of the unstrained Ge control devices. Finally, we explain the observed enhancement and degree thereof in terms of the various factors addressed above.

4.2 ADAPTATION OF MCUT TO STUDY STRAINED GE PMOSFETS

In our paper [Gho05] we summarized the modifications made to our 2-D Monte Carlo device simulator, MCUT in order to study Ge MOSFETs. In order to study strained Ge, we calculated the strained Ge valence band structure using the tight binding method [Vog83]. In particular, for strained Ge on $\text{Si}_{0.3}\text{Ge}_{0.7}/\text{Si}$ (as considered in [Rit03]) the lattice constants in the plane of the biaxial strain and perpendicular to it are 5.5775 Å and 5.6992 Å respectively as opposed to the relaxed Ge lattice constant of 5.646 Å. This corresponds to a biaxial strain of 1.2 %. Acoustic and optical phonon scattering rates were calculated from the full band structure using Fermi's Golden Rule [Wan93]. The coupling (deformation) potentials for strained Ge were taken to be the same as those for unstrained Ge and they are 1.0 eV for acoustic phonons and 8.0 eV/Å⁰ for optical phonons as obtained from a matching of empirical velocity versus field data (for holes in unstrained Ge) shown in Figure 4.1.

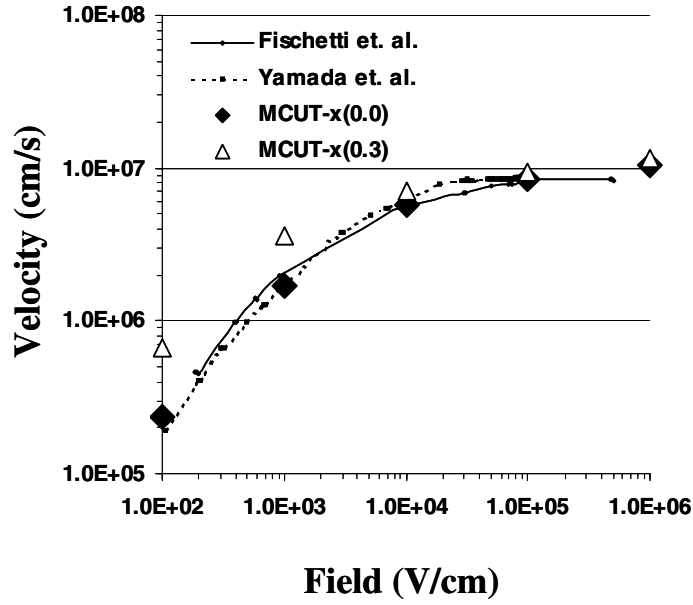


Figure 4.1: MCUT data on velocity versus field for holes in unstrained Ge and strained Ge (x denotes the mole fraction of Si in the buffer layer) and comparison with literature data.

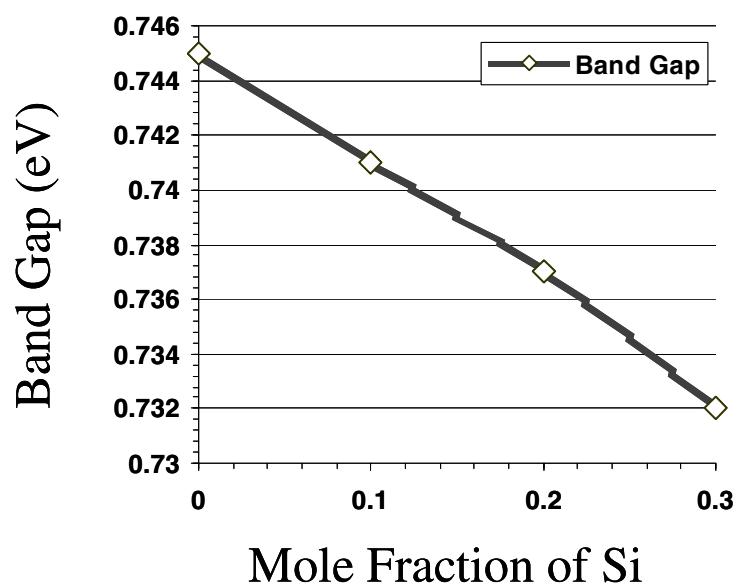


Figure 4.2: Band gap of strained Ge as a function of the mole fraction of Si in the $\text{Si}_x\text{Ge}_{1-x}$ buffer layer.

Impact ionization, ionized impurity scattering and surface roughness scattering are also modeled. The band gap of strained Ge changes as a function of strain as shown in Figure 4.2 and the appropriate band gap (for a Si mole fraction of 0.3) was used in the impact ionization formula. We used the same parameters of impurity scattering for unstrained Ge and strained Ge.

The surface roughness parameters L , ΔZ and α have been tuned for holes to match experimental mobility versus effective field data in [Rit03] for strained Ge (Ge on $\text{Si}_{0.3}\text{Ge}_{0.7}/\text{Si}$) with HfO_2 as gate oxide as shown in Figure 4.3 and Table 4.1. Due to lack of data in the literature, at the present time, we use the same surface roughness parameters for strained and unstrained Ge with HfO_2 as gate oxide.

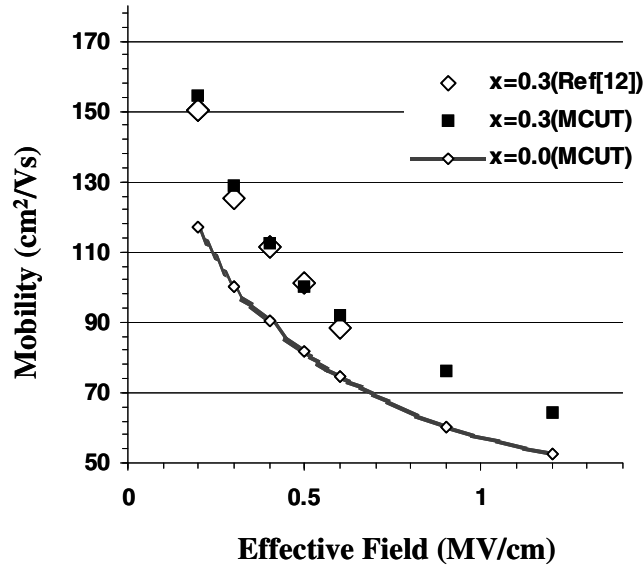


Figure 4.3: Mobility versus Effective Field comparison of PMOSFETs in unstrained Ge and strained Ge (x denotes the mole fraction of Si in the buffer layer) with HfO_2 as gate oxide.

Parameter/Material (oxide)	$L(\text{\AA})$	$\Delta Z (\text{\AA})$	α	$m_{\text{dos}}(m_0)$
Ge(HfO ₂)	20.0	34.53	0.795	0.26(x=0.3) 0.44(x=0.0)

Table 4.1: Parameters of surface roughness scattering for strained and unstrained Ge PMOSFETs with HfO₂ as gate oxide. Here x denotes the Si mole fraction in the buffer layer.

Our valley-dependent quantum corrections (and only the corrections) are obtained within an effective mass approximation [Rav00]. Since the hole bands are highly non parabolic even in the range of equilibrium carrier distributions, consideration of the band curvature at only the Γ -point can be misleading. Instead we obtain the effective mass from a Boltzmann-weighted average of the local band curvature,

$$\frac{\hbar^2}{m_{\text{perp}}} = \frac{\int \frac{\partial^2 E(\mathbf{k})}{\partial k_{\text{perp}}^2} \exp\left(-\frac{E(\mathbf{k})}{k_B T}\right) d^3 \mathbf{k}}{\int \exp\left(\frac{E(\mathbf{k})}{k_B T}\right) d^3 \mathbf{k}} \quad (4.1)$$

where m_{perp} and k_{perp} denote the effective mass and wave vector respectively normal to the interface. The strained Ge hole quantization effective mass values for quantization in the $\langle 001 \rangle$ direction are obtained from Eq. 4.2 and the strained Ge bandstructure. Also, the 2-D (in the plane of transport, $m_{\text{2d-dos}}$) density of states masses used for quantum correction have been calculated from the quantization masses and the 3-D density-of-states-masses ($m_{\text{3d-dos}}$) according to the following formula,

$$m_{\text{2d-dos}} = \sqrt{\frac{m_{\text{3d-dos}}^3}{m_{\text{Quantization}}}} \quad (4.2)$$

such that the correct 3-D density of states is obtained in the weak confinement limit. The values of the various masses used for strained and unstrained Ge used in this study are given in Table 4.2.

Band/Mass(m_0)	Hole band		
	Heavy hole	Light hole	Split-off hole
Quantization mass along (001)	0.457(x=0.3) 0.305(x=0.0)	0.136(x=0.3) 0.064(x=0.0)	0.058(x=0.3) 0.078(x=0.0)
3-d density-of-states mass	0.252(x=0.3) 0.410(x=0.0)	0.040(x=0.3) 0.104(x=0.0)	0.042(x=0.3) 0.072(x=0.0)
2-d density-of-states mass	0.187(x=0.3) 0.475(x=0.0)	0.022(x=0.3) 0.132(x=0.0)	0.036(x=0.3) 0.068(x=0.0)
Conductivity mass along (100)	0.540(x=0.3) 0.305(x=0.0)	0.079(x=0.3) 0.064(x=0.0)	0.107(x=0.3) 0.078(x=0.0)

Table 4.2: Values of quantization and density-of-states-masses used for strained and unstrained Ge. Here x denotes the Si mole fraction in the buffer layer.

4.3 DEVICE SIMULATION RESULTS

Device simulations were performed on 50 nm channel length PMOSFETs. These device structures were constructed (for simulation purpose) similar to that in [Ant99] and

have a 2 nm thick gate oxide, substrate doping of $1 \times 10^{15} \text{ cm}^{-3}$, and with {100} surface orientations and <100> transport directions. HfO_2 was used as the gate oxide. The PMOSFET had a p^+ source/drain region with a Gaussian doping distribution with a peak density of $2 \times 10^{20} \text{ cm}^{-3}$, and a p^+ polySi gate of 85 nm physical length (with a doping of $2 \times 10^{20} \text{ cm}^{-3}$ and height of 60 nm). Figure 4.4 shows the I_D vs. V_D curves for strained and unstrained Ge PMOSFETs (with HfO_2 as gate oxide) at $V_G - V_{th} = -1.0 \text{ V}$. The drive current enhancement in the strained Ge device over its unstrained Ge counterpart at $V_D = -1.2 \text{ V}$ is about 41%. As pointed out in [Lun97],[Pal04], scattering near the source channel barrier plays the main role in determining the on current of nanoscale MOSFETs. The effective transverse fields corresponding to the peak position of the source-channel barrier (which is about 55 nm from the source contact in the direction of the channel for both strained and unstrained Ge) were $0.729 \times 10^6 \text{ V/cm}$ and $0.716 \times 10^6 \text{ V/cm}$, respectively, for the strained and unstrained Ge devices. These effective fields correspond to low-field mobilities of $88 \text{ cm}^2/\text{Vs}$ and $51 \text{ cm}^2/\text{Vs}$ for the strained and unstrained Ge devices, respectively, as obtained from simulation of long channel devices at low drain voltages and shown in Figure 4.3. This corresponds to an enhancement in mobility of about 66 %. Thus a significant advantage of strained Ge comes from its higher mobility than that of unstrained Ge.

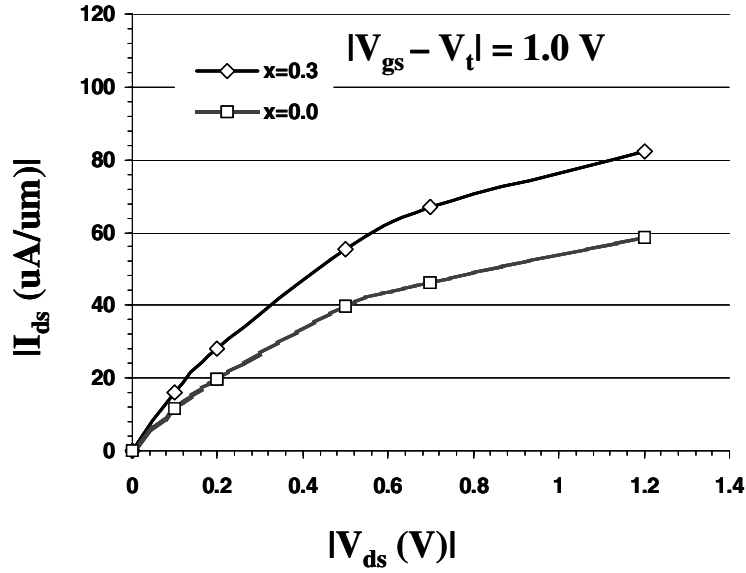


Figure 4.4 Comparison of drain current versus drain voltage characteristics for 50 nm strained Ge (x denotes the mole fraction of Si in the buffer layer) and unstrained Ge PMOSFETs. The surface and channel directions are along [001] and [100], respectively. The values of currents and voltages are negative but the absolute values of these quantities have been plotted. The gate oxide used is HfO_2 for both strained Ge and unstrained Ge.

4.4 DISCUSSION

Biaxial strain in Ge causes a splitting of the heavy and light hole bands at the Γ point and the splitting increases with increasing levels of strain as shown in Figure 4.5. For a biaxial strain of 1.2 % (corresponding to a Si mole fraction of 0.3 in the buffer layer) the splitting (calculated from our bandstructure) is about 96 meV as shown in Figure 4.5, ($\sim 3.7 k_B T$ at room temperature) with the heavy hole band having lower

energy than the light hole band. In addition, the split off band energy increases from 295 meV for unstrained Ge to 390 meV for strained Ge. These increases in energy separations between the hole bands reduce the interband scattering rate as shown in figure 4.6. Although the effective masses of holes increase slightly due to strain as shown in figures 4.7 and 4.8, the low field hole mobility increases (due to the lower scattering rate) from 1689 cm²/Vs for unstrained Ge to 3645 cm²/Vs for 1.2% biaxially strained Ge, an increase of about 116 % in accordance with the results in [Fis96]. The dependence of low field mobility of strained Ge on the Si mole fraction is shown in Figure 4.9.

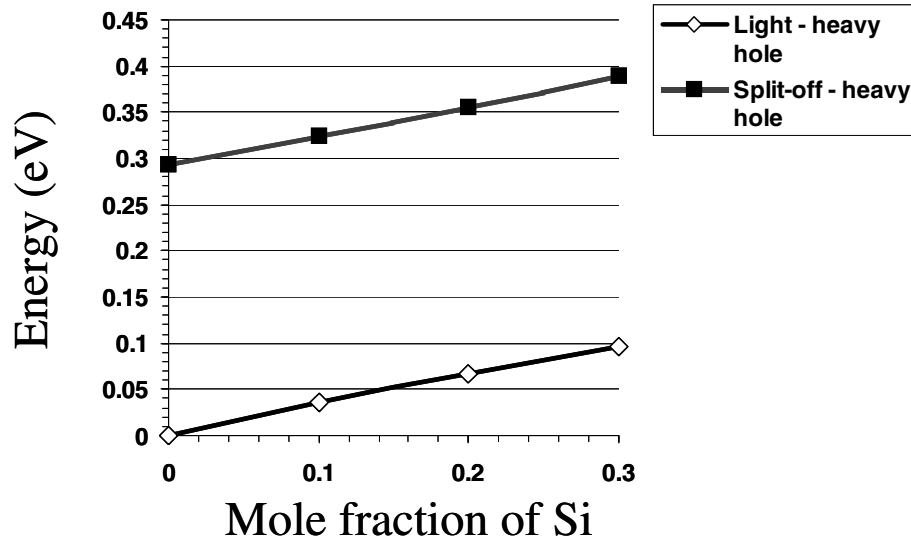


Figure 4.5: Energy splitting between the light hole and heavy hole bands and the split-off hole and heavy hole bands as a function of the mole fraction of Si in buffer layer.

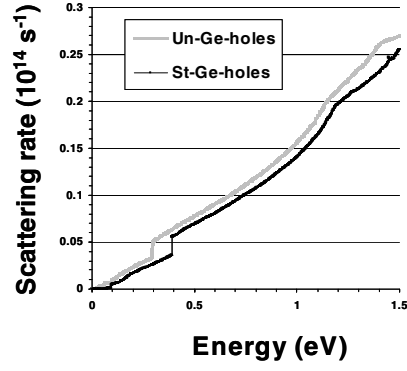


Figure 4.6: Phonon scattering rates of holes in strained and unstrained Ge.

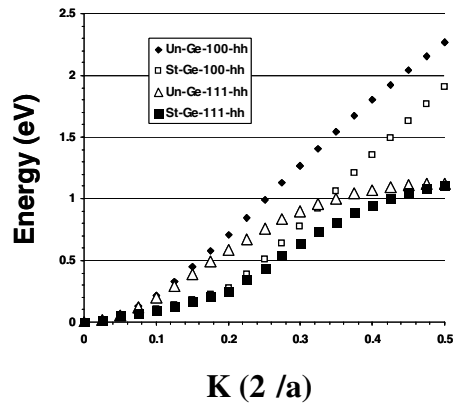


Figure 4.7: Heavy hole bandstructure of strained and unstrained Ge along (100) and (111) directions.

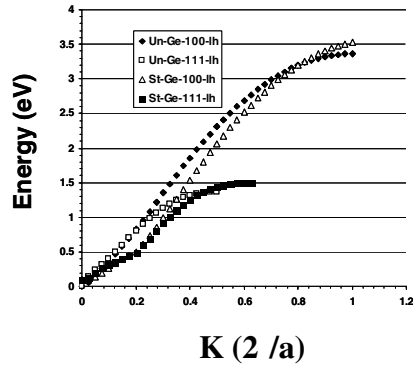


Figure 4.8: Light hole bandstructure of strained and unstrained Ge along (100) and (111) directions.

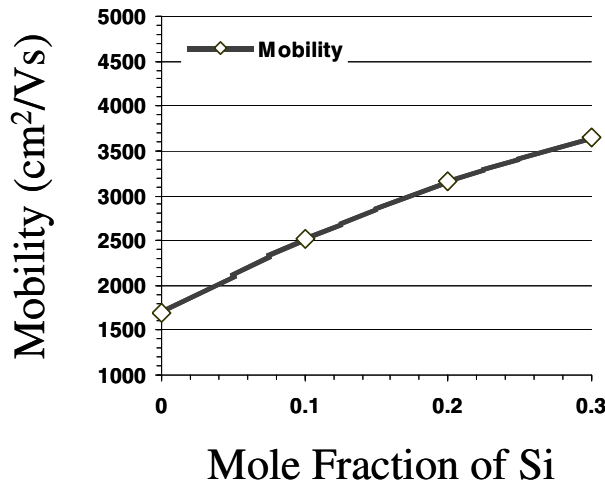


Figure 4.9: Low field mobility of holes in strained Ge (as a function of the mole fraction of Si).

The low field mobility improvement of holes in strained Ge over those in unstrained Ge can be attributed to reduced interband scattering. However, for holes, the surface roughness scattering plays a critical role in channel mobilities, reducing the relative mobility increase for strained Ge over unstrained Ge in the inversion channel as compared to that in bulk.

The increase in drive current of 41 % for the 50 nm P-channel device, is substantially smaller than the increase in mobility enhancement of about 66 %. It is thermal velocity that limits the injection current in the ballistic limit [Lun97]. For these simulations of short channel devices and nearly equal thermal velocities for holes of strained and unstrained Ge, for the employed full band structure, much of the advantages of the increased mobilities are lost.

Furthermore, Figure 4.10 compares the velocity profiles along the entire length including the source, the channel and the drain for the 1.2% strained Ge and unstrained Ge 50nm PMOSFETs. As pointed out in [Lun97], increased carrier velocity further down

the channel including any velocity overshoot of the carriers in the channel does not extend the limit of the saturation current. However, the significant velocity overshoot and increment in average velocity in the channel does improve transit times through the device which can be related to signal delay and RF performance, [Fie99]. In this respect strained Ge has an advantage over unstrained Ge as well.

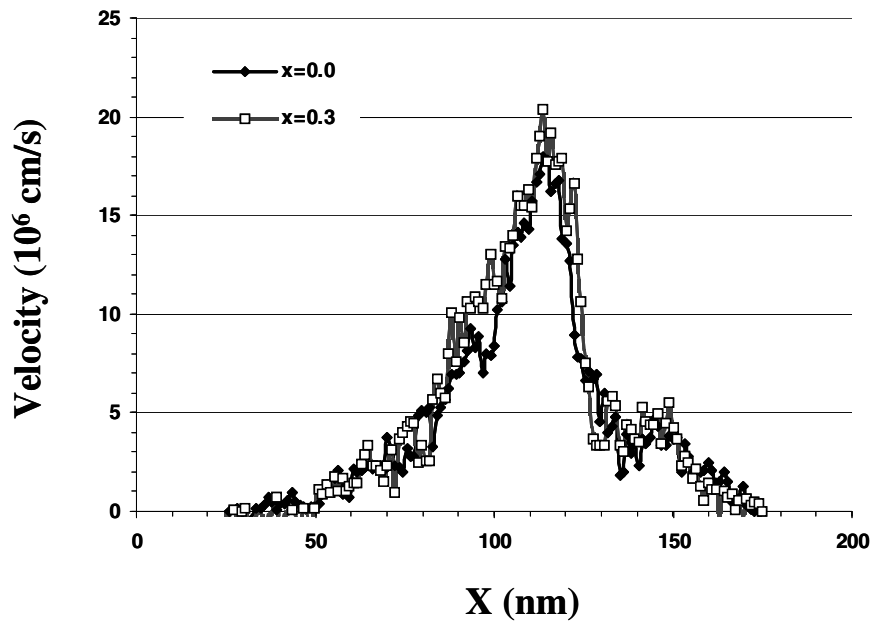


Figure 4.10: Velocity profile from source to drain in 50 nm channel length unstrained Ge and strained Ge (x denotes the mole fraction of Si in the buffer layer) PMOSFETs. The entire MOSFET extends from 25 nm to 175 nm. The channel is of effective length 50 nm and extends from about 75 nm to about 125 nm.

Chapter 5: REMOTE SCATTERING IN GE PMOSFETS

5.1 MOTIVATION

As the channel length in CMOS (Complementary Metal-Oxide Semiconductor) devices continues to be scaled down, so must the thickness of the dielectric in order to control short channel effects. However, when the thicknesses of conventional dielectrics, like SiO_2 , used in Si MOSFETs are reduced below 2 nm, the gate leakage current (due to direct tunneling) becomes prohibitively high ($> 1\text{A}/\text{cm}^2$ for a gate voltage of 1.0V) for low standby power applications. This impediment to gate oxide scaling has led to the interest in high- κ dielectrics as possible replacements for conventional (low- κ) dielectrics like SiO_2 . For the same gate capacitance, the physical thickness of the high- κ dielectrics can be almost an order of magnitude higher than that of SiO_2 thereby reducing the gate leakage current by several orders of magnitude. However, the integration of high- κ dielectrics on Si is challenging for several reasons, including flatband and threshold (V_t) voltage shifts and V_t instabilities due to fixed charges and charge trapping in the high- κ film, and degradation of carrier mobility in the channel. The issue of degradation of carrier mobility is particularly important and several alternative materials to Si, such as strained SiGe, strained Si and unstrained and strained Ge have recently been considered for channel mobility improvement. Ge seems to be a particularly interesting candidate due to its considerably higher electron (2X) and hole (4X) bulk mobility than Si.

Although the use of Ge with high- κ can counterbalance the problem of reduced channel mobility experienced with high- κ in Si devices to some extent, the same mechanisms that cause the reduction of channel mobility in Si MOSFETs exist in their Ge counterparts and reduce the mobility relative to a high quality gate dielectric on Ge MOSFET. In order to obtain the greatest benefits from device scaling, it is, therefore, necessary to identify these mobility-degrading mechanisms in high- κ -on-Ge MOSFETs and reduce their effect on device performance to the maximum possible extent.

Recently several experimental and theoretical studies have been performed to understand the nature and strength of the mobility degrading mechanisms in thin dielectrics (with or without high- κ) on Si and Ge N- and PMOSFETs [Liu87],[Sai04]. In particular, in the pioneering work in [Liu87] it was shown that the remote surface roughness limited mobility decreases with decrease in the dielectric thickness (t_{ox}), and the technique in [Liu87] was used in [Sai04] to explain the experimentally observed hole mobility reduction with decrease in t_{ox} in Al_2O_3 on Si transistors. In another work [Luj03] a model of remote Coulomb scattering capable of predicting the effects of an arbitrary charge distribution in the gate dielectric was proposed and tested on experimental data on electron mobility in HfO_2 -on-Si transistors. The influence on the channel mobility of electrons of remote charge scattering from depletion charge in the polycrystalline Si gate was examined in [Sai02][Sol04][Gam03]. In another comprehensive work [Rol03], an improved theory of remote-charge-scattering-limited mobility in Si inversion layers taking into account the effects of image charges, screening and interface trapped charges was developed and incorporated in a Monte Carlo simulator, and it was shown that remote Coulomb scattering of channel electrons cannot be neglected for dielectric effective thicknesses below 2 nm.

However, to the best of our knowledge, there has been no theoretical Monte Carlo study on the performance degradation due, simultaneously, to remote Coulomb and remote surface roughness scattering mechanisms in ultra-thin high- κ -on-Ge PMOSFETs. In this chapter we describe a full band Monte Carlo study on the effects of remote Coulomb and remote surface roughness scattering on the performance of nanoscale bulk Ge PMOSFETs. We first show that the experimentally observed data on the dependence of mobility on the thickness of high- κ dielectrics can be explained by scattering due to remote surface roughness at the gate-dielectric interface and remote Coulomb scattering due to fixed charges in the dielectric, and then investigate the performance degradation of Ge PMOSFETs due to these scattering mechanisms. Besides remote Coulomb and remote surface roughness scattering, in our simulations, we consider transport including phonon, ionized impurity, surface roughness (at the oxide-channel interface) scattering and impact ionization. Carrier redistribution in real space and among energy valleys (k -space) due to quantum confinement within the inversion layer is addressed via position and valley/band-dependent quantum-corrected potentials.

The chapter is organized as follows. We first describe the modifications made to MCUT in order to take into account remote Coulomb and remote surface roughness scattering. Next we present our results on the performance degradation due to remote Coulomb and remote surface roughness scattering mechanisms in Ge bulk PMOSFETs. Finally we explain the observed degradation and degree thereof in terms of the various factors addressed above.

5.2 ADAPTATION OF MCUT TO STUDY REMOTE SURFACE ROUGHNESS AND REMOTE COULOMB SCATTERING

The scattering rates of remote surface roughness scattering and remote Coulomb scattering have been implemented in MCUT following equation 2.9 and 2.12, respectively. The final state (wavevector) selection is done (for simplicity) similarly for normal surface roughness and remote surface roughness scatterings (as also similar final state selection methods are used for normal impurity scattering and remote Coulomb scattering). For surface roughness scattering, the final wavevector is randomized and for impurity scattering the final wavevector is chosen according to Ridley's impurity scattering rate. The mobilities are calculated by doing a long channel MOSFET simulation and obtaining the ratio of the average velocity to the average field, the average being taken over all the particles in the ensemble. The result of the fitting is shown in Figure 5.1 and the values of surface roughness, surface phonon, remote surface roughness and remote Coulomb scattering are given in Table 5.1.

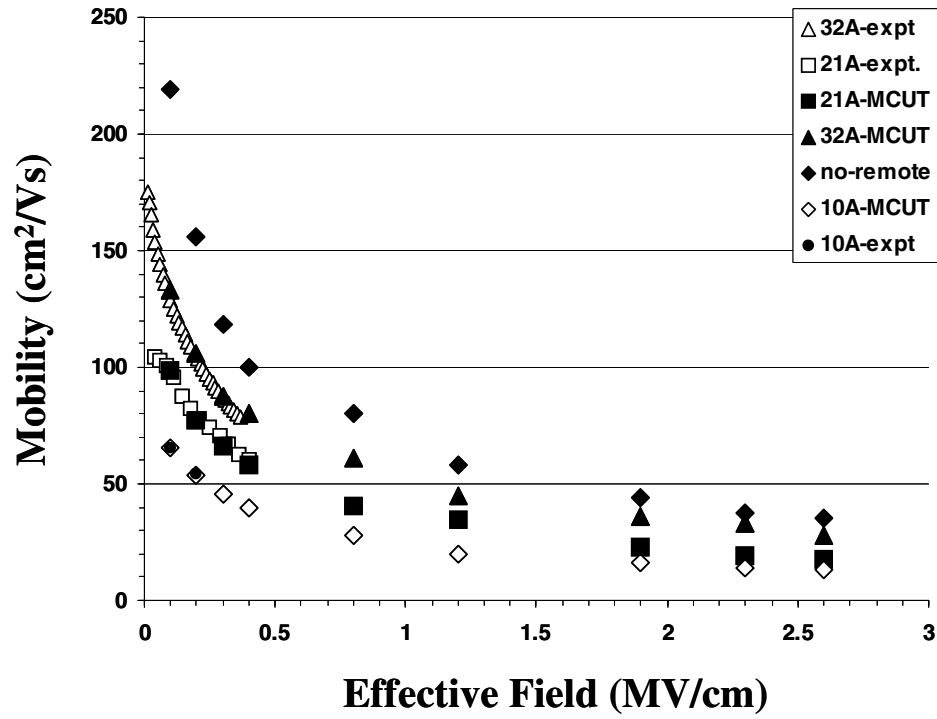


Figure 5.1: Experimental and MCUT data on mobility versus effective field as a function of oxide thickness.

L(nm)	$\Delta Z(\text{nm})$	α	$R(\text{s}^{-1}\text{V}^{-1}\text{cm})$	β	$L_1(\text{nm})$
2.0	17.9	0.3	81.751×10^6	1.0	2.0
$\Delta Z_1(\text{nm})$	$C_{\text{RSR}}(\text{cm}^{-6}\text{s}^{-1}\text{eV}^{-1/2})$	α_1	$C_{\text{RC}}(\text{cm}^{-3}\text{s}^{-1}\text{eV}^{-1/2})$	$t_s(\text{nm})$	$t_e(\text{nm})$
2.0	1.63×10^{49}	0.3	3.8×10^{39}	0.5 ($t_{\text{ox}}=2.1 \text{ nm}$ and 3.2 nm)	1.0 ($t_{\text{ox}}=2.1 \text{ nm}$) 0.8 ($t_{\text{ox}}=3.2 \text{ nm}$)

Table 5.1: Values of parameters used in surface roughness, remote surface roughness and remote Coulomb scattering mechanisms for unstrained Ge.

The values of the various quantization effective masses (refer to equations 4.1 and 4.2) used for unstrained Ge used in this study are given in Table 5.2. As detailed in [Fan04], these values are then used in effective-mass-based quantum mechanical calculation of the total carrier density as a function of position within the quantum-confined system. The band edges for the semiclassical 3-D calculations of MCUT are then shifted to provide the same carrier density.

Material/Mass(m_0)	Unstrained Ge		
	Heavy hole	Light hole	Split-off hole
Quantization mass along (001)	0.2995	0.0622	0.0786
3-d density-of-states mass	0.43	0.014	0.025
2-d density-of-states mass	0.515	0.007	0.0141
Conductivity mass along (100)	0.2995	0.0622	0.0786

Table 5.2: Values of quantization and density-of-states masses used for unstrained Ge.

5.3 DEVICE SIMULATION RESULTS

The experimental mobilities were extracted from a self-isolated ring Ge PMOSFET with two mask layers, the gate pattern mask and the source-drain contact pattern mask with isolation obtained by tying the source ring to the ground. The

PMOSFETs were fabricated using (100) n-type Ge wafers of resistivity 0.1 ohm-cm and a self aligned MOSFET process. Tungsten was used as the gate material and Al for the source-drain contacts. Ultrathin HfO₂ of varying thicknesses (t_{eq} ranging from 1.0 to 3.2 nm) were deposited using UHV reactive atomic beam deposition.

The effective mobility was calculated using long channel MOSFETs (channel length 100 μ m) at low lateral fields using the gradual channel approximation

$$\mu_{eff}(V_g) = I_d / [(W / L)V_d Q_{inv}(V_g)] \quad (5.1)$$

where the inversion charge density Q_{inv} was calculated using the split C-V method as follows :

$$Q_{inv}(V_g) = \int C_{gc}(V_g) dV_g \quad (5.2)$$

where C_{gc} is the gate-to-channel capacitance per unit area and the integration over V_g is performed from accumulation to inversion. The extracted mobility is plotted as a function of the effective field given by

$$E_{eff} = (Q_B + 1/2 Q_{inv}) / \epsilon_{Ge} \quad (5.3)$$

where Q_B is the substrate charge density and ϵ_{Ge} is the permittivity of Ge. The resultant mobility versus effective field data is shown in Figure 5.1 for oxide thicknesses of 2.1 and 3.2 nm.

Device simulations were performed on 50 nm channel length single gate PMOSFETs. The MOSFETs were constructed (for simulation) similar to that in [Ant99] with a 2.0 nm thick gate oxide, substrate doping of $1 \times 10^{15} \text{ cm}^{-3}$, and with (100) surface orientations and [100] transport directions. These devices have a p+ source/drain region with a Gaussian doping distribution with a peak density of $2 \times 10^{20} \text{ cm}^{-3}$, and a p+ polySi

gate of 85 nm physical length (with a doping of $2 \times 10^{20} \text{ cm}^{-3}$ and height of 60 nm). Figure 5.2 shows the I_D vs. V_D curves for the Ge PMOSFET with and without remote scattering at $V_G - V_t = -1.0 \text{ V}$ and -0.5 V . The decrease in the saturation current due to remote scattering at $V_G - V_t = -1.0 \text{ V}$ is 15.3 % and at $V_G - V_t = -0.5 \text{ V}$ is 16.7 %. The effective fields at the peak of the source-channel barrier in the single gate device and the corresponding mobilities obtained from simulation of long channel devices at low drain voltages are mentioned in Table 5.3. The distances of the peaks from the contacts at the source ends are 55 nm for the single gate MOSFETs.

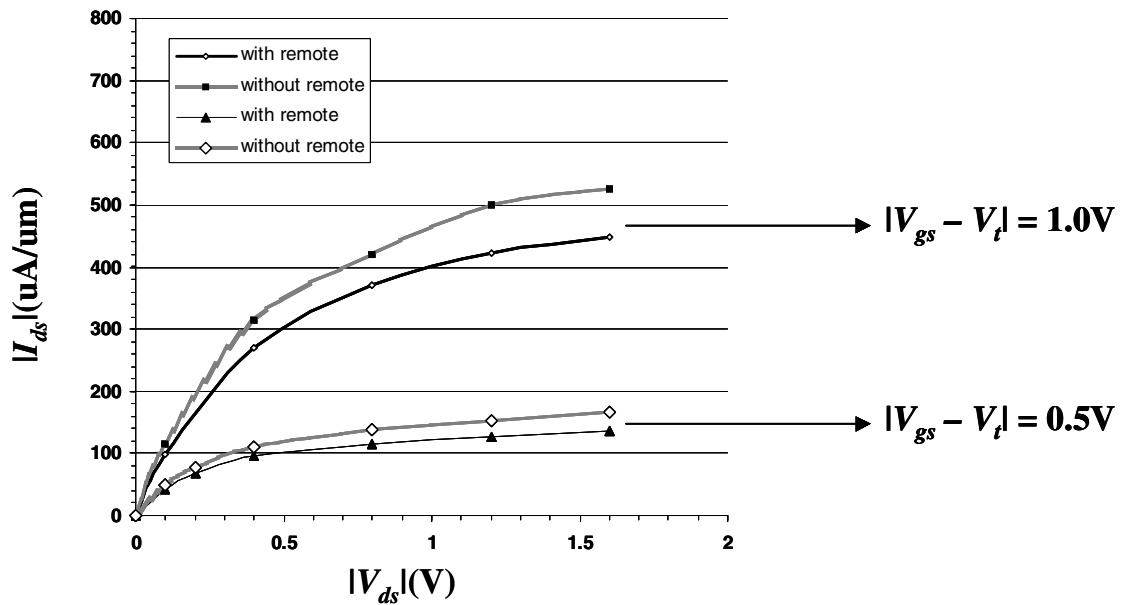


Figure 5.2: Drain current versus drain voltage curves for various gate overdrives, ($V_G - V_t$), for 50 nm Ge bulk (single gate) PMOSFETs with and without remote scattering.

Device/scattering	50 nm single gate PMOSFET	
	$V_g - V_t = -1.0$ V	$V_g - V_t = -0.5$ V
With remote scattering	1.22×10^6 (32.6)	8.27×10^5 (40.2)
Without remote scattering	1.24×10^6 (59.3)	8.38×10^5 (80.23)

Table 5.3: Effective fields (in MV/cm) and mobilities (in cm^2/Vs) at the peak of the source-channel barrier for single gate 50 nm PMOSFET at various ($V_g - V_t$) and with and without remote scattering in the format effective field (mobility).

5.4 DISCUSSION

Figure 5.1 shows the experimental results on the dependence of the mobility on the effective field for various oxide thicknesses. The parameters of the remote scattering mechanisms were obtained by fitting the simulation results from MCUT with those obtained from experiments, and the result of the fitting and the values of the parameters are shown in Figure 5.1 and Table 5.1, respectively. As evident from our results (shown

in Figure 5.2), remote scattering (including both remote Coulomb and remote surface roughness) plays an important role in nanoscale Ge PMOSFETs reducing the saturation current by as much as 16%. As discussed in [Lun97], the mobility at the peak of the source-channel barrier still plays an important role in determining the saturation currents of nanoscale MOSFETs. Therefore, we obtained the values of the effective field and mobility at the peak of the source-channel barrier, as shown in Table 5.3. The values thus obtained for the mobility, qualitatively, correspond well with the observed values of the saturation current. For example at $V_g - V_t = -1.0$ V, the effective fields at the peak of the source channel barrier are 1.22×10^6 MV/cm with remote scattering and 1.24×10^6 MV/cm without remote scattering, almost if not quite the same. However, the corresponding mobilities, obtained from Figure 5.1, are $32.6 \text{ cm}^2/\text{Vs}$ and $59.3 \text{ cm}^2/\text{Vs}$, respectively. This corresponds to a decrease of 45.0% in mobility and of 15.3% in saturation current (as shown in Figure 5.2) due to remote scattering. Similar trends between mobility at the peak of the source-channel barrier and saturation current are obtained at other gate voltages for the single gate MOSFET. As obtained in our simulations, and consistent with available experimental data, the difference in the mobilities between cases with and without remote scattering increases as the effective field is reduced. Figure 5.3 shows the dependence of the mobility (in the presence of remote scattering) as a function of oxide thickness at different values of the effective field. Although the relative importance of remote surface roughness and remote coulomb scattering decreases at higher E_{eff} as discussed above, for the E_{eff} of ~ 1.2 MV/cm found in the on state in our simulations these scattering processes will remain important for (effective oxide thickness), $t_{\text{eq}} < \sim 3$ nm that will be encountered in such devices. This result is similar to that obtained for Si [Gam03][Rol03].

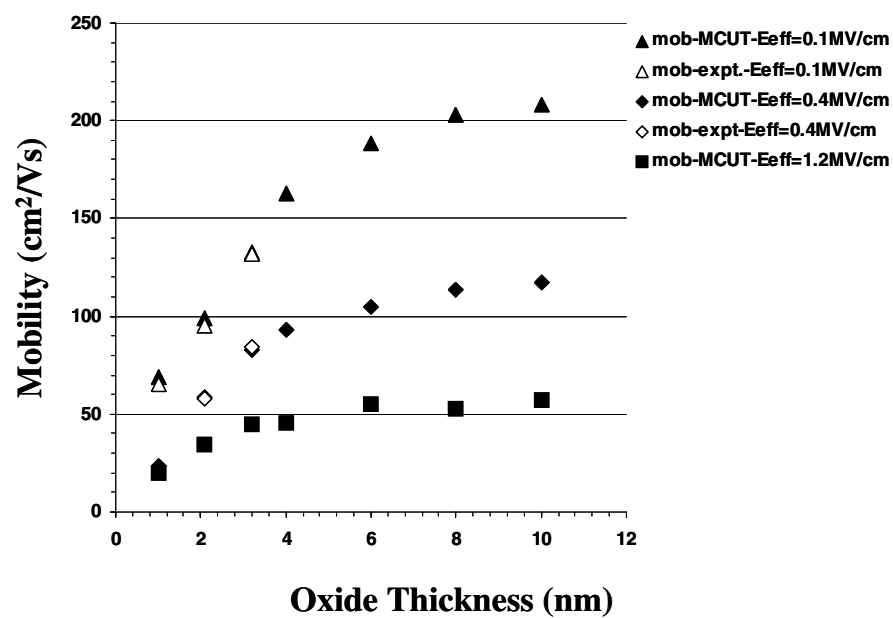


Figure 5.3: MCUT results for mobility as a function of oxide thickness for various effective fields.

Chapter 6: CHANNEL LENGTH SCALING STUDY OF STRAINED AND UNSTRAINED GE PMOSFETS

6.1 MOTIVATION

In Chapter four, we discussed strain induced mobility enhancement in Ge PMOSFETs for a channel length of 50 nm. However, with the continuous shrinking of device sizes, it is not obvious that the improvement in hole mobility of strained Ge over unstrained Ge will result in higher saturation currents for shorter channel lengths as well where thermal velocities are more important [Lun97]. In [Buf03] it was shown, by single particle, fullband Monte Carlo simulations, that this results in the reduction in the saturation current enhancement of strained Si over unstrained Si as the channel length of the PMOSFET is reduced. In this chapter, we perform a full band Monte Carlo study of strained Ge PMOSFETs and compare with their unstrained Ge counterparts for various effective channel lengths (L_{eff}) ranging from 50 nm down to 30 nm. The chapter is organized as follows: We first present the results of our simulations of strained (Ge on $Si_{0.3}Ge_{0.7}/Si$) Ge PMOSFETs and compare the results with those of the unstrained Ge control devices for channel lengths ranging from 50 nm to 30 nm. Then, we explain the observed degradation in saturation current enhancement due to channel length scaling in terms of the various factors addressed above.

6.2 DEVICE STRUCTURE AND SIMULATION RESULTS

The bandstructures and scattering rates of holes in strained and unstrained Ge were obtained following the lines discussed in chapter four. Device simulations were performed on three PMOSFETs with effective channel lengths ranging from 50 nm down to 30 nm. The 50 nm channel length MOSFET was constructed (for simulation purpose) similar to that in [Ant99] and has a 2 nm thick gate oxide, substrate doping of $1 \times 10^{15} \text{ cm}^{-3}$, and with {100} surface orientations and <100> transport directions. HfO_2 was used as the gate oxide. The PMOSFET has a p^+ source/drain region with a Gaussian doping distribution with a peak density of $2 \times 10^{20} \text{ cm}^{-3}$, and a p^+ polySi gate of 85 nm physical length (with a doping of $2 \times 10^{20} \text{ cm}^{-3}$ and height of 60 nm). The other MOSFET structures were obtained from the 50 nm structure by scaling the channel length (to 40 nm and 30 nm) and keeping the oxide thicknesses constant at 2 nm. The channel dopings in the MOSFETs were tuned to match the threshold voltages with unstrained Si channels. The values are $N_D = 1.0 \times 10^{15} \text{ cm}^{-3}$, $1.5 \times 10^{16} \text{ cm}^{-3}$, $1.7 \times 10^{17} \text{ cm}^{-3}$ for the 50 nm, 40 nm and 30 nm PMOSFET, respectively.

Figure 6.1 shows the I_D vs. V_D curves for strained and unstrained Ge PMOSFETs (with HfO_2 as gate oxide) at $V_G - V_{th} = -1.0 \text{ V}$ for the smallest (30 nm) simulated MOSFET. The enhancement in saturation current at $V_D = -1.2 \text{ V}$ and $V_G - V_t = -1.0 \text{ V}$ is about 21 %. Figure 6.2 shows the saturation current as a function of the channel length for the unstrained and strained Ge PMOSFETs and Figure 6.3 shows the ratio of the saturation current of strained Ge PMOSFET to that of the unstrained Ge PMOSFET as a function of channel length. The saturation currents are measured at the same gate overdrive, $V_G - V_{th}$, of -1.0 V and drain voltage, V_D , of -1.2 V for the strained and unstrained PMOSFETs with various channel lengths.

We observe that although the absolute values of the saturation currents increase with reduction in the channel lengths for both the strained and unstrained Ge channels, the ratio of the saturation currents of strained Ge to that of unstrained Ge decreases as the channel length is reduced.

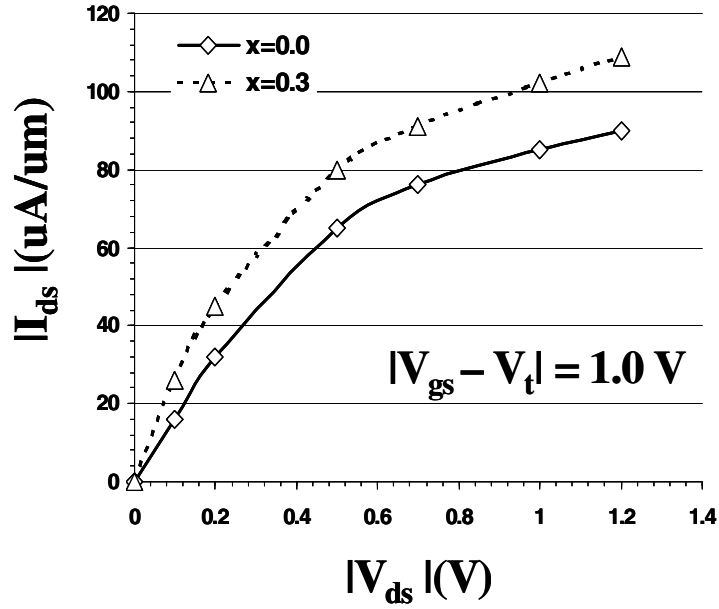


Figure 6.1: Comparison of drain current versus drain voltage characteristics for 30 nm strained Ge (x denotes the mole fraction of Si in the buffer layer) and unstrained Ge PMOSFETs.

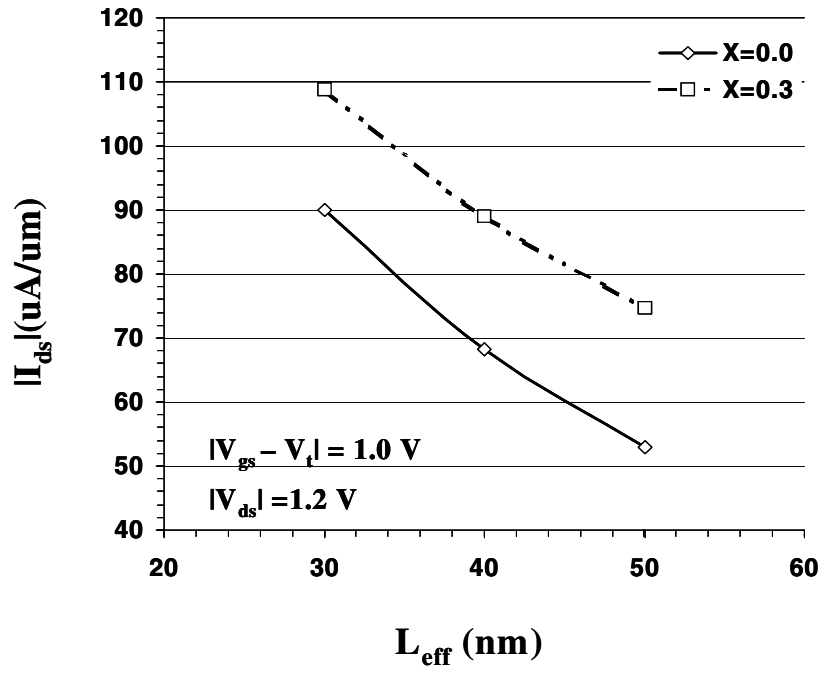


Figure 6.2: Dependence of saturation current as a function of channel length from 50 nm down to 30 nm for strained and unstrained Ge PMOSFETs (x denotes the mole fraction of Si in the buffer layer).

6.3 DISCUSSION

Biaxial strain in Ge causes a splitting of the heavy and light hole bands at the Γ point and increases the split-off band energy, as discussed in chapter four. These increases in energy separations between the hole bands reduce the density of states at low energies as shown in Figure 6.4 and hence decrease the scattering rate. As discussed in chapter four, the increase in saturation current of strained Ge over unstrained Ge can be understood by somewhat measuring the mobility of carriers at the peak of the source channel barrier which is higher for strained Ge than for unstrained Ge giving rise to the higher drain current in the former.

To understand the device simulation results for various channel lengths, we show in Figures 6.5 and 6.6 the electric field and velocity of holes as function of position along the channel with origin taken at the peak of the source channel barrier (where the longitudinal field is zero). The field profile shows that as the channel length is reduced, the electric field near the source end increases for both the strained and unstrained cases. According to Figure 4.1, this should result in increased velocities near the source and this is correctly reflected in Figure 6.6.

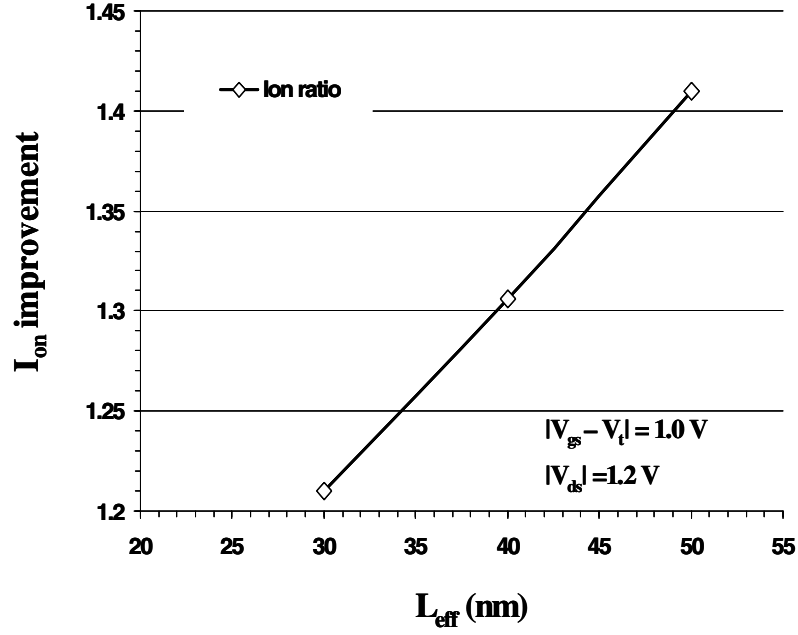


Figure 6.3: Ratio of ON currents of strained (Si mole fraction of 0.3 in the buffer layer) and unstrained Ge PMOSFETs as a function of channel lengths from 30 nm to 50 nm.

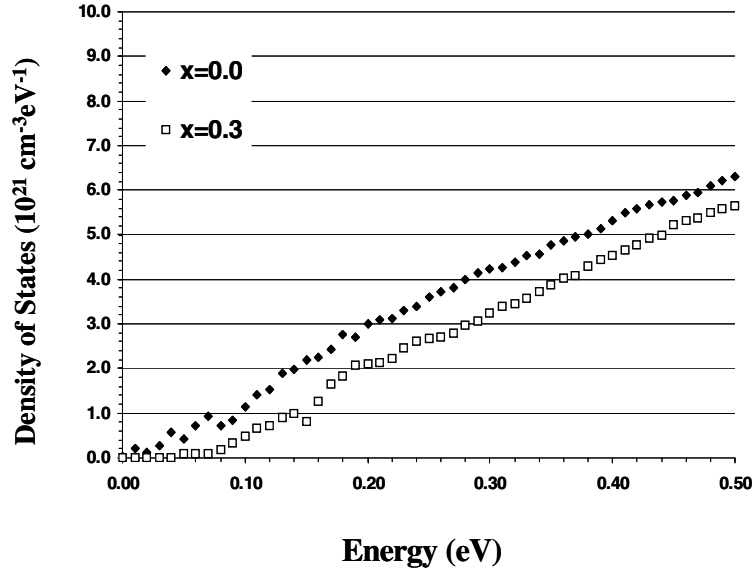


Figure 6.4: Comparison of low energy density of states of holes in strained and unstrained Ge (x denotes the mole fraction of Si in the buffer layer).

As explained in [Ban00], the velocity of carriers at the source end determines the on current of MOSFETs and this is reflected in Figure 6.2 where the on current increases as the channel length is reduced or equivalently the electric field near the source end is increased.

To understand the strain dependence of the on current, we note from Figure 4.1 that the improvement in velocity due to strain decreases as the electric field is increased. Correspondingly, for shorter channel lengths (or equivalently as the electric field near the source end increases), the improvement in carrier velocities near the source end due to strain decreases resulting in decreased ratio of the ON currents of strained-to-unstrained cases, as observed in Figure 6.3.

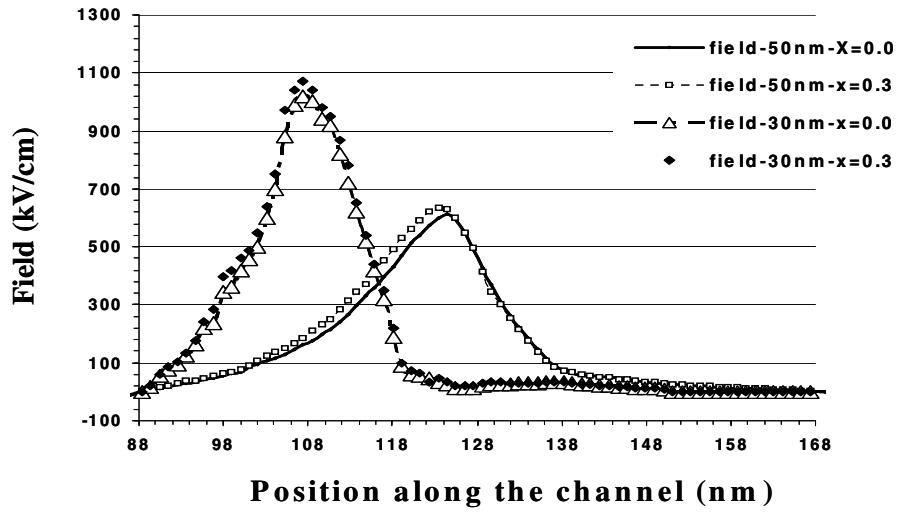


Figure 6.5: Profile of the electric field from source to drain in 50 nm and 30nm channel length unstrained Ge and strained Ge (x denotes the mole fraction of Si in the buffer layer) PMOSFETs. The origin is taken at the peak of the source channel barrier.

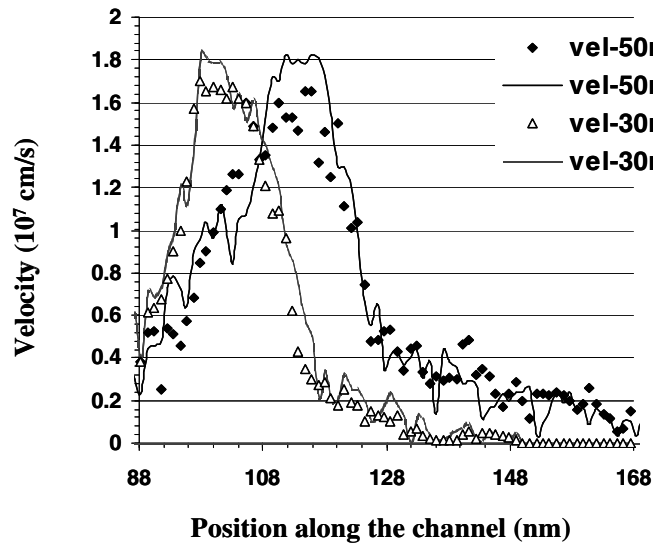


Figure 6.6: Velocity profile of carriers from source to drain in 50 nm and 30 nm channel length unstrained Ge and strained Ge (x denotes the mole fraction of Si in the buffer layer) PMOSFETs. The origin is taken at the peak of the source channel barrier.

Chapter 7: ORIENTATION STUDY OF UNSTRAINED SI NMOSFETS

7.1 MOTIVATION

The drive currents of MOSFETs can be enhanced by using crystal orientations other than the (100) substrate [Mom02]. The PMOS and NMOS devices can be fabricated with different surface orientations like {100}, {110} and {111} and with different orientations of the channel directions like $\langle 111 \rangle$, $\langle 112 \rangle$, $\langle 110 \rangle$ and $\langle 100 \rangle$, [Hwa04], [Shi89]. The PMOS ($L_g = 45$ nm) can have 30% improvement in drive current for the channel along the $[1\bar{1}0]$ direction on a (110) substrate as compared with the channel $[1\bar{1}0]$ on (001) substrates. The highest electron mobility with oxynitride gate dielectric is reported along the [011] direction on the (100) substrate. The highest hole mobility is observed for a [011] channel on a (100) substrate. At the inversion charge density of $\sim 6 \times 10^{12} \text{ cm}^{-2}$, the hole mobility of $[1\bar{1}0]/(110)$ devices is increased by 160 % as compared with the $\langle 110 \rangle/(001)$ device, [Yan03]. Channel directions affect both the hole and electron mobilities dramatically on (110) substrate but relatively little on (111) substrate. The orientation dependence of mobility is caused by the anisotropy of the bandstructure combined with the effects of quantum confinement.

In this chapter, we study the surface orientation dependence of drive currents of Si NMOSFETs by Monte Carlo simulations. The chapter is organized as follows. We first describe the method used to study the orientation dependence. Then we present the results on drain current versus drain voltage on 50 nm channel length Si NMOSFET for different orientations. Finally, we explain the results.

7.2 METHODOLOGY

In a MOSFET, the orientation between the coordinate systems of the crystal and the device can, in general, be arbitrary. The crystal coordinate system is defined along the (100) equivalent directions and the device coordinate system is defined along the transport, quantization and width directions. Some physical quantities are defined better in device coordinate system, like the carrier concentration, the potential etc. while others, like the bandstructure and scattering rates are stored in the crystal coordinate system. In MCUT we perform a general transformation between these two coordinate systems by using Euler angles. The electric field a carrier experiences is first obtained in the device coordinate system by a solution of the Poisson equation with the known carrier concentration in the device and the applied terminal voltages on the MOSFET. The particles are moved by this electric field. The resulting particle momentum is mapped to the crystal coordinate system to obtain the particle velocity and scattering rates. After scattering and final state selection in the crystal coordinate system the final momentum of the particle is mapped back to the device coordinate system. The velocity when mapped back to the device coordinate system leads the real space position of the particle at the

end of the flight. We schematically illustrate this mapping technique between the two coordinate systems in figure 7.1.

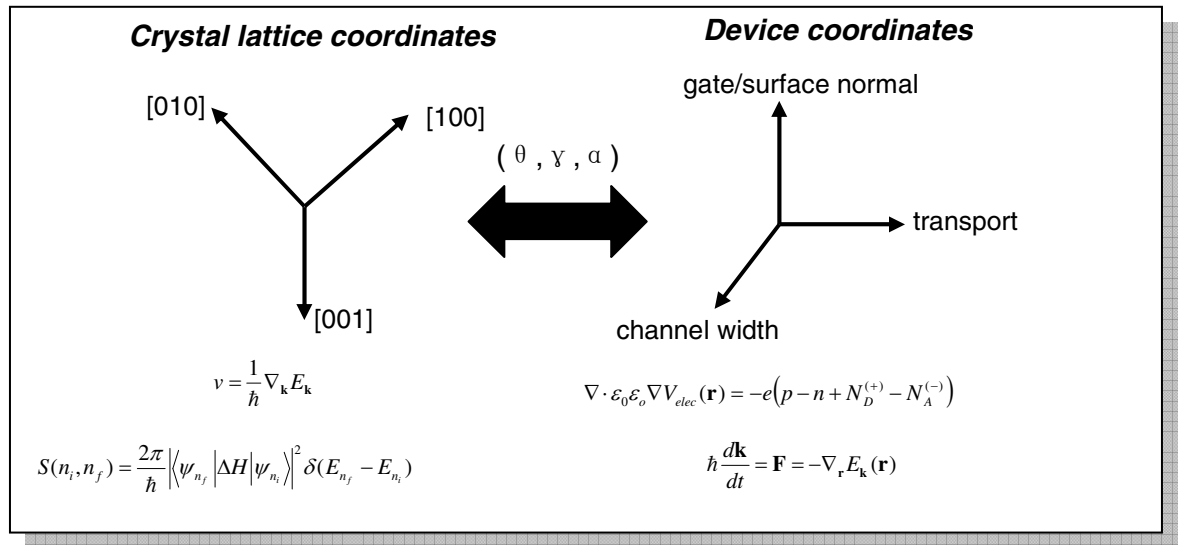


Figure 7.1: The mapping of relevant physical quantities between the crystal and device systems.

We perform device simulations on 50 nm MIT well tempered MOSFET structure. In addition to the various scattering models (like, phonon, ionized impurity, surface roughness scattering and impact ionization), quantum correction is taken into account. The quantization mass depends on the orientation of the oxide-Si surface and the values are tabulated in Table 7.1.

Surface orientation	Valley _{degeneracy} (material)	2-D DOS mass	Quantization mass
(001)	• ₂ (Si)	0.19	0.97
	• ₄ (Si)	0.44	0.19
(110)	• ₄ (Si)	0.34	0.33
	• ₂ (Si)	0.44	0.19
(111)	• ₆ (Si)	0.38	0.27

Table 7.1: Quantization and 2-D density of states masses for various surface orientations of electrons in Si.

The results of the device simulations are plotted in figure 7.2. In these simulations, we assume identical surface roughness parameters for all the orientations.

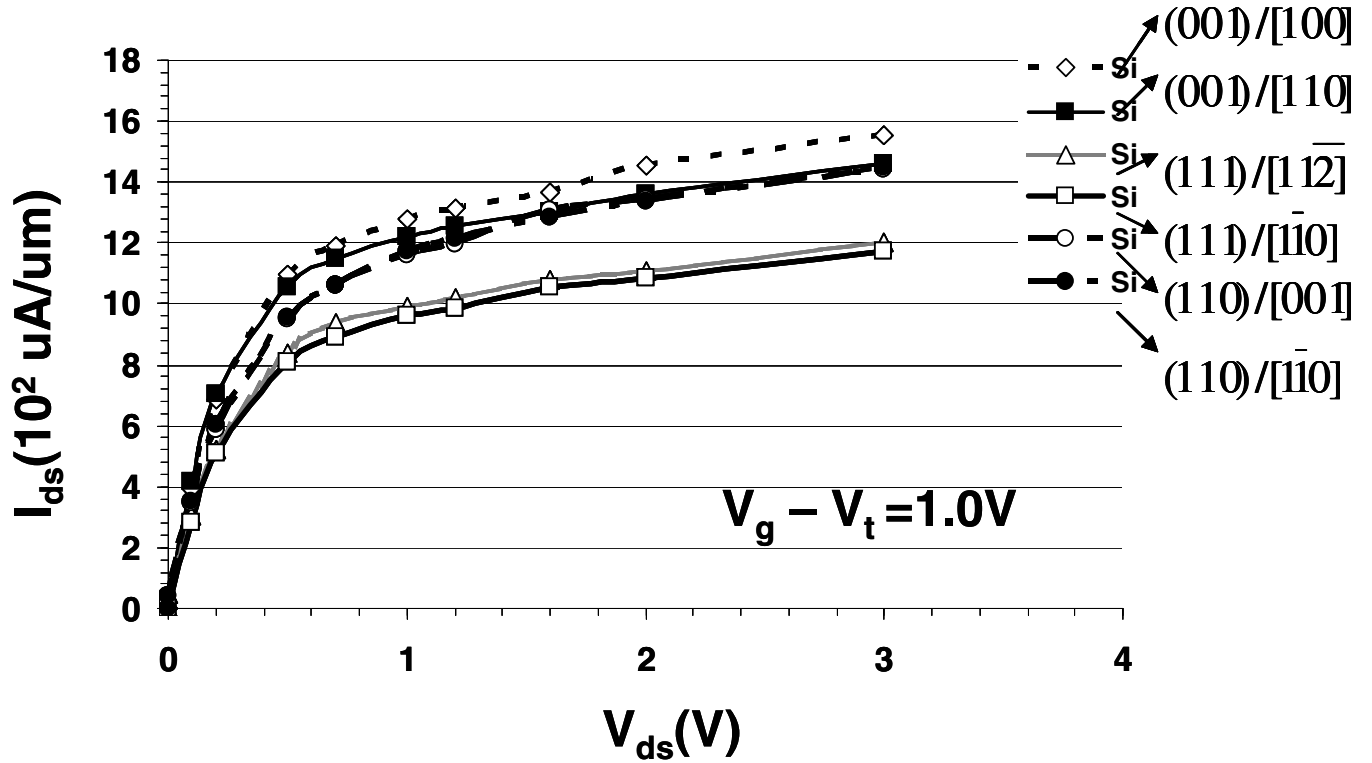


Figure 7.2: Drain current versus drain voltage for various wafer and transport directions in the notation (wafer direction)/[transport direction].

7.3 DISCUSSION

Figure 7.2 shows that for Si NMOSFETs, the (100) surface gives the highest drive current, followed by the (110) surface. To understand this behaviour, we look at table 7.2. It is obvious that the (100) surface corresponds to the largest separation in the quantization masses of the \bullet_2 and \bullet_4 valleys of Si compared to any of the other surfaces. Hence larger numbers of carriers settle in the \bullet_2 valley of the (100) surface oriented Si

NMOSFET. In addition, the conductivity effective mass of electrons for the (100) surface is the smallest when compared with other surfaces. Hence the inversion layer mobility is the highest for the (100) wafer direction. Since the drive current is a monotonic function of the mobility, the drive current is the highest for the (100) surface.

Chapter 8: STUDIES ON III-V SEMICONDUCTORS

8.1 MOTIVATION

We discussed in the previous chapters that as the gate lengths of complementary metal oxide semiconductor field effect transistors (CMOSFETs) are being scaled down to increase chip density and reduce cost, new challenges have emerged that need to be dealt with. The very high channel doping concentration and reduced dielectric thickness needed to obtain good short channel behavior also cause reduced mobility in the channel and increased gate leakage current. While gate leakage current can be reduced by introducing high-k materials as the dielectric, this further reduces channel mobility and the drive current suffers. Hence the focus is on improving the saturation currents by introducing higher-mobility channel materials replacing conventional Si channels. Recently, III-V semiconductors have generated significant interest in the electronic industry as possible replacement for Si, particularly, due to the much high electron mobility in III-V compared to Si.

Several experimental and theoretical studies have been made on III-V semiconductor devices. In [Che84], a self aligned recessed gate InP MESFET with high transconductance has been described. In another interesting work, [Dat05], a 85 nm gate length enhancement and depletion mode InSb quantum well transistor suitable for high speed and very low power logic applications has been demonstrated. Besides, in [Cha05], planar III-V compound semiconductor (InSb, InAs, etc.) FETs were benchmarked against Si transistors at about 100 nm gate length regime and possible advantages in terms of

reduced gate delay in the III-V FETs were exhibited. In [Guo04], properties of Wurtzite GaN MESFETs of 0.4 μm gate length have been studied by two dimensional fullband Monte Carlo approach and its potential as a high frequency and high power device has been reported. In another study, [Her05], Monte Carlo simulations are performed on nanoscale InSb FETs and the effect of impact ionization on the high speed performance of these MOSFETs has been investigated. In an interesting paper [Rah05], performance limits of unstrained n- and p- MOSFETs with Si, GaAs and InAs channel materials were investigated using a semi-empirical tightbinding model and a top-of-the barrier semi numerical ballistic transport model and it was observed that the III-V semiconductors underperform identical Si n type transistors despite the higher electron mobility in the former. In another work, [Fis91-1], Monte Carlo studies with nonparabolic bandstructures for III-V semiconductors and without quantum correction were performed on short channel III-V transistors and the dependence of the transconductance on the channel material was discussed.

However, to the best of our knowledge, no comparative theoretical Monte Carlo study taking into account fullband structure and quantum correction of nanoscale III-V transistors with their Si counterparts have, so far, been attempted. In this chapter we perform a preliminary fullband semiclassical Monte Carlo study of III-V NMOSFETs (made of GaAs and InP) and compare with their Si counterparts. In our simulations, we consider transport including phonon and surface roughness scattering and impact ionization. Carrier redistribution in real space and among energy valleys (k-space) due to quantum confinement within the inversion layer is addressed via position and valley/band-dependent quantum-corrected potentials.

This chapter is organized as follows: We start with a brief discussion of the modifications made to MCUT in order to study III-V NMOSFETs. Next we present the results of our simulations of nanometer channel length III-V NMOSFETs and compare the results with those of unstrained Si control devices.

8.2 GAAS AND INP NMOSFETs

In the following, we briefly describe the modifications made to the existing version of MCUT to allow simulation of III-V channel material devices. The bandstructure and the phonon scattering rate table are obtained from the same preprocessing programs as in the Si version, with tight-binding parameters obtained from [Vog92]. The deformation potentials for phonon scattering have been tuned to obtain reasonable agreement with data from the literature [Lev95],[Sze47]. The data considered include velocity versus field for electrons in Si and III-V semiconductors, as shown in Figure 8.1. The values of the acoustic longitudinal (ϵ_{LA}), acoustic transverse (ϵ_{TA}) and optical (ϵ_{op}) deformation potentials used for electrons in this study are given in Table 8.1. (The given values of the deformation potentials, however, are not unique in their ability to match the experimental velocity-field and other sets of values can be used.) Due to the lack of experimental data the surface roughness parameters L and ΔZ have been chosen to be identical for Si and III-V MOSFETs and are taken to be $L = 22\text{\AA}$, $\Delta Z = 1.78\text{\AA}$, $\alpha = 2.0$. The values of m_{dos} used are mentioned in Table 8.2. The parameters of polar optical phonon scattering including the nonparabolicity factor, β , the effective mass, m_{dos} is the effective mass, the optical phonon energy ϵ_{op} and the high frequency and static dielectric constants κ_{∞} and κ_o , respectively are mentioned in Table 8.2. The

quantization effective masses of Si and III-V semiconductors used are the 3D density of states effective masses and they are also mentioned in Table 8.2.

Deformation potential / Material	$\Delta_{LA}(\text{eV})$	$\Delta_{TA}(\text{eV})$	$\Delta_{OP}(\text{eV/cm})$
Si	3.54	1.49	$5.6 \cdot 10^8$
InP	4.0	4.0	$8.0 \cdot 10^8$
GaAs	0.1	0.1	$8.0 \cdot 10^8$

Table 8.1: Acoustic longitudinal, acoustic transverse and optical phonon deformation potentials for Si, InP and GaAs.

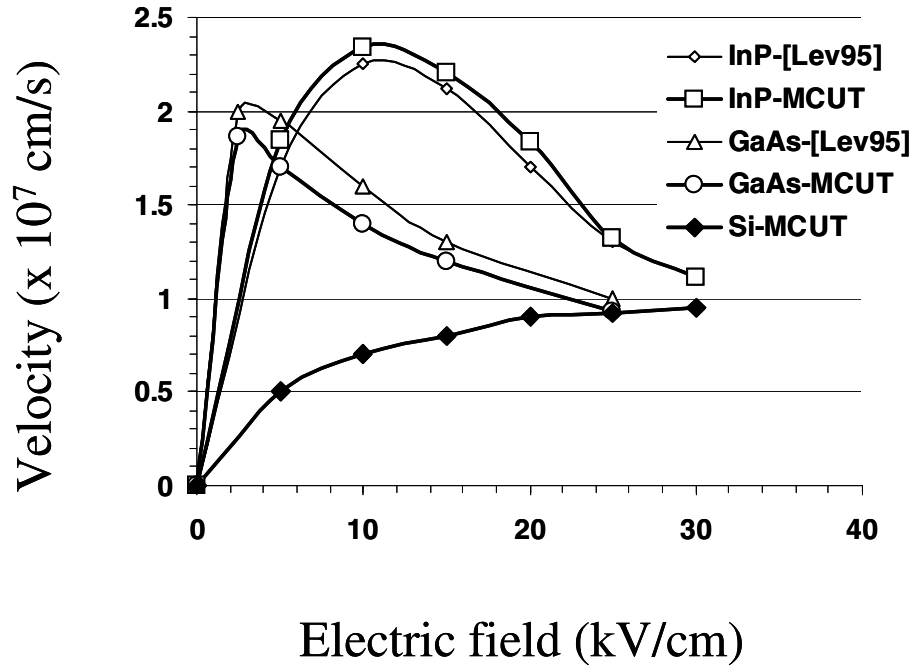


Figure 8.1: MCUT data on velocity versus field for electrons in unstrained Si, InP and GaAs and comparison with literature data.

	$m_{\text{dos}}(m_0)$	$\omega_{\text{OP}}(\text{meV})$	k_{∞}	k_o	$\alpha (\text{eV}^{-1})$
Si	0.36	63		11.7	
InP	0.08	43	9.61	12.5	0.627
GaAs	0.063	35	10.9	12.9	0.616

Table 8.2: Density-of-states-mass, optical phonon energy, dielectric constant and non-parabolicity factor for electrons in Si, InP and GaAs. m_0 denotes free electron mass.

8.3 DEVICE SIMULATION RESULTS

Device simulations were performed on NMOSFETs of Si, GaAs and InP. The Si channel NMOSFET was constructed (for simulation purpose) similar to that in [Ant99] and has a 2 nm thick gate oxide, substrate doping of $1 \times 10^{15} \text{ cm}^{-3}$, and with {100} surface orientations and <100> transport directions, n^+ source/drain region with a Gaussian doping distribution with a peak density of $2 \times 10^{20} \text{ cm}^{-3}$, and a n^+ polysilicon gate of 85 nm physical length (with a doping of $2 \times 10^{20} \text{ cm}^{-3}$ and height of 60 nm). SiO_2 was used as the gate oxide. The effective channel length, defined as the distance between the metallurgical p-n junctions at the source and drain ends, of this MOSFET is 37 nm. For GaAs and InP, source drain doping concentrations of $2 \times 10^{20} \text{ cm}^{-3}$ are unrealistic and even if possible are detrimental to device performance due to the occupation of higher effective mass L and X valleys at such high dopings, [Fis91-2]. The source drain dopings were therefore reduced by an order of magnitude to $2 \times 10^{19} \text{ cm}^{-3}$ for GaAs and InP and the device structure was adjusted to obtain an effective channel length of 37 nm according to the definition given above.

Figure 8.2 shows the I_d vs. V_d curves for Si, GaAs and InP NMOSFETs at $V_G - V_{th} = -1.0 \text{ V}$. The degradation in saturation current (compared to Si) at $V_d = 1.2 \text{ V}$ and $V_G - V_{th} = 1.0 \text{ V}$ is about 21 % for InP and 52 % for GaAs. We consider our results to be preliminary.

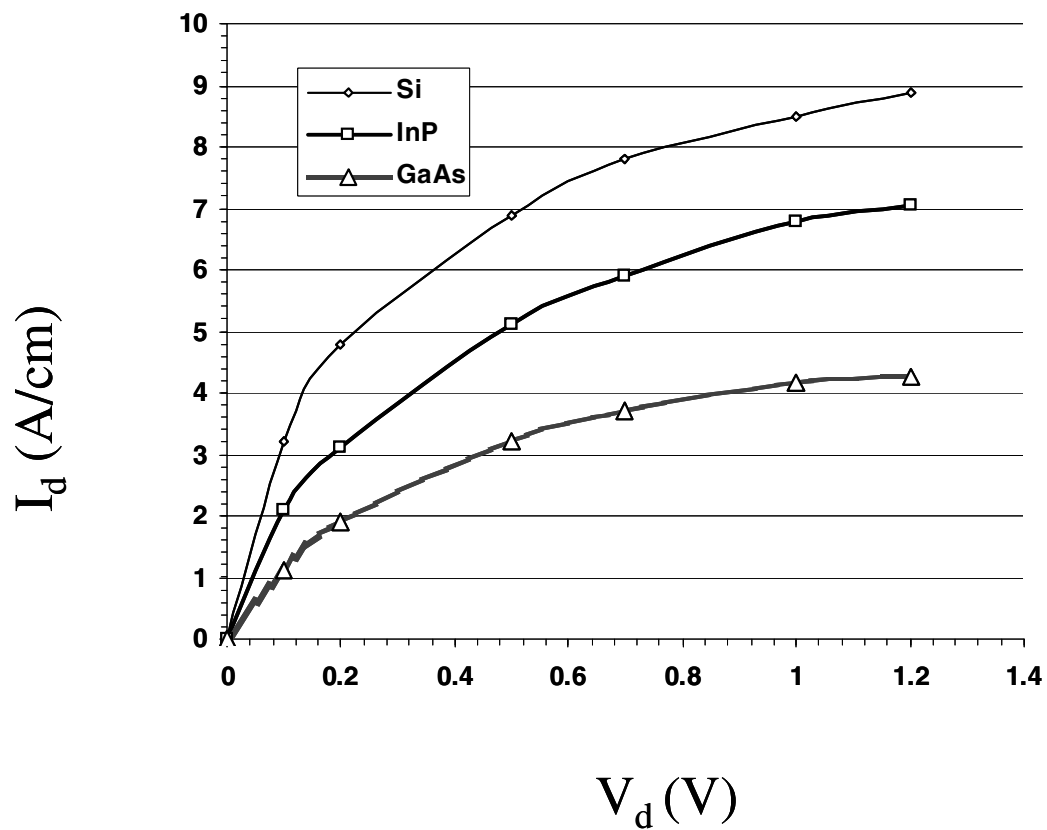


Figure 8.2: Drain current versus drain voltage for a gate overdrive voltage of 1.0 V for 37 nm channel length Si, InP and GaAs NMOSFETs.

In order to explain these preliminary results, we show in Table 8.3 the inversion charge densities and average velocities of carriers near the peak of the source channel barrier for Si, InP and GaAs NMOSFETs at threshold and at a gate voltage of 1.0 V above threshold. It is observed that the inversion charge densities of InP and GaAs are lower than those in Si. To understand this, we first consider the threshold condition. The threshold voltage has been obtained by keeping a constant drain voltage of 1.2 V and by tuning the gate voltage such that the drain current is about $1 \mu\text{A}/\mu\text{m}$. Because of the higher mobilities of electrons in InP and GaAs compared to that in Si, the electron velocities are higher in the former. Hence the inversion charge densities are less for the III-V MOSFETs so that the same current (of $1 \mu\text{A}/\mu\text{m}$) is obtained at threshold. As the gate voltage is increased to about 1.0 V above threshold, quantum correction effectively reduces the gate capacitance by pushing the inversion charge away from the interface and thus reduces the inversion charge density. The lower quantization effective masses of the III-V semiconductors amplifies this effect and the result is a lower inversion charge density in the III-V MOSFETs. The product of the inversion charge density and carrier injection velocity is a measure of the drain current in MOSFETs and their values for Si and the III-V MOSFETs have been given in Table 8.3. Clearly, the III-V MOSFETs have a lower value of this product and this gets reflected in their lower drain currents.

Although, in this work, simulations were performed without taking Fermi statistics into account, we note that the inclusion of Fermi statistics resulting in the exclusion principle will exacerbate the situation for the III-V MOSFETs. For, the substantially lower conduction band densities in these materials will imply much lower

inversion charge densities in the ON state of the MOSFETs and hence lower ON currents. We expect that simulations including Fermi statistics will shed more light on these preliminary results.

	Si	InP	GaAs
Sheet charge(cm^{-2}) (Q, $V_g-V_t=1.0\text{V}$) (Q, $V_g-V_t=0.0\text{V}$) (NQ, $V_g-V_t=1.0\text{V}$) (NQ, $V_g-V_t=0.0\text{V}$)	1.853×10^{13} 1.299×10^{10} 2.849×10^{13} 3.11×10^{10}	4.152×10^{12} 1.0075×10^{10} 6.93×10^{12} 1.522×10^{10}	2.75×10^{12} 5.78×10^9 4.00×10^{12} 8.27×10^9
Velocity (cm/s) (Q, $V_g-V_t=1.0\text{V}$) (Q, $V_g-V_t=0.0\text{V}$) (NQ, $V_g-V_t=1.0\text{V}$) (NQ, $V_g-V_t=0.0\text{V}$)	6.01×10^6 8.22×10^6 4.93×10^6 6.5×10^6	2.207×10^7 1.26×10^7 2.058×10^7 1.5144×10^7	1.95×10^7 2.0127×10^7 1.75×10^7 2.47×10^7
Velocity x Sheet charge($\text{cm}^{-1}\text{s}^{-1}$) (Q, $V_g-V_t=1.0\text{V}$) (Q, $V_g-V_t=0.0\text{V}$) (NQ, $V_g-V_t=1.0\text{V}$) (NQ, $V_g-V_t=0.0\text{V}$)	11.14×10^{19} 10.68×10^{16} 14.05×10^{19} 20.2×10^{16}	9.75×10^{19} 12.7×10^{16} 14.26×10^{19} 23.05×10^{16}	5.36×10^{19} 11.62×10^{16} 7.00×10^{19} 20.42×10^{16}

Table 8.3: Inversion charge density and average velocity of electrons near the peak of the source channel barrier for 37 nm channel length Si, InP and GaAs NMOSFET with (Q) and without (NQ) quantum correction.

Chapter 9: CONCLUSIONS AND RECOMMENDATIONS

9.1 CONCLUSIONS

We modified an existing semiclassical Monte Carlo simulator (MCUT) to study alternative channel materials such as Ge and III-V (GaAs and InP) semiconductors. New scattering mechanisms such as remote surface roughness and remote Coulomb scattering that become predominant in high-k materials have been implemented. Polar optical phonon scattering has been implemented to study III-V semiconductors. We employed full band structure to study the material properties of Ge, GaAs and InP.

Despite the high (phonon limited) low field mobility of Ge compared to Si, the ON current suffers because of the high surface roughness and impurity scattering in threshold-voltage-matched Ge and Si MOSFETs. Strained Ge PMOSFETs perform better than unstrained Ge PMOSFETs but not so much as to significantly outperform strained Si PMOSFETs. Integration of high-k on Ge PMOSFETs reduces the on current significantly due to the mobility degrading scattering mechanisms such as remote surface roughness and remote Coulomb scattering. GaAs and InP NMOSFETs perform worse than their Si counterparts due to the lower conduction band densities of states in the III-V semiconductors compared to that in Si.

9.2 RECOMMENDATIONS

The study of III-V semiconductors can be extended to materials other than GaAs and InP, e.g. GaN, InSb etc. Currently, the code considers Boltzmann statistics. However, the III-V semiconductors have low conduction band density of states and hence become highly degenerate under usual dopings of the order of $1 \times 10^{19} \text{ cm}^{-3}$. Fermi statistics should, therefore, be used.

For high-k dielectrics, soft phonon scattering is an important phenomenon and should be implemented. The final state selection process in remote surface roughness and remote Coulomb scatterings have been implemented according to that in normal surface roughness and Ridley's impurity scattering. This can be improved to account for the actual scattering probability of the remote scattering mechanisms. Impurity scattering has been implemented analytically in the code. This can be improved to consider full band structure. Carrier carrier scattering should also be implemented.

In quantum confinement, the effective potential method used currently handles the electron band structure well. Modifications to effectively handle hole bandstructure are still required.

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